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MULTILAYER ELECTRET ACTIVATED BY DIRECT CONTACT SILICON ELECTRODE

by

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B.S.M.E., Purdue University, 1991
M.S.E.E., University of Louisville, 1999

A Dissertation
Submitted to the Faculty of the
JB Speed Engineering School of the University of Louisville
In Partial Fulfillment of the Requirements
For the Degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering
University of Louisville
Louisville, Kentucky

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DEDICATION

This dissertation is dedicated to my family

Angie, Wyatt, and Andrew.

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ABSTRACT

MULTILAYER ELECTRET ACTIVATED BY DIRECT CONTACT SILICON ELECTRODE

Mark M Crain III

November 11, 2014

Electrets used in microelectromechanical systems (MEMS) devices are often formed by corona charging, where ionized gases are generated in an electric field to introduce a charge to the electret surface. The purpose of this study was to investigate a new technique for creating an electret from a plasma enhanced chemical vapor deposition (PECVD) multilayer film of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ using a direct contact electrode of silicon. The electret formation takes advantage of deep traps in silicon nitride, which are known to develop from hydrogen interactions with silicon dangling bonds and, in some stoichiometries, nitrogen dangling bonds. The electret activation process has been optimized for maximum effective surface voltage (ESV). The deposition and activation process for the electret has the additional benefit of using commercially available equipment present in many microelectronic fabrication facilities. Standardized processes for depositing the PECVD film stack and activating the electret with a wafer level bonder have been developed.

Using this new process, electret films have been produced with positive and negative effective surface voltages in excess of ± 194.0 V. Extrapolated lifetimes, based on thermal decay studies, are calculated to be 57 years and 23 years for positive and negative electrets respectively if they are maintained in moderate to low humidity environments below 125°C . Activation energy levels in positive and negative electrets are 1.4 eV and 1.2 eV respectively. This new electret multilayer film stack and direct charging method produced thin film electrets with a half-life 5 times greater than that reported in literature by other groups using PECVD multilayer electrets [1, 2].

A new application was investigated to see how an electret may benefit semiconductor-liquid interactions. The PECVD electret was used to apply a gate bias to the back side of a double side polished silicon wafer to determine the effect of gate bias on the etch rates of an anisotropic silicon etch in 25% wt. tetramethylammonium hydroxide (TMAH). Our results show that the positively charged electret produced a statistically significant increase in etch rate, when compared to neutral and negatively charged electrets, as the silicon-TMAH interface approached the depletion region produced by the electret. The mean values of the silicon etch rate were evaluated for the last hour of etching with samples categorized by electret potentials as positive, negative or neutral. The positive potential electret had a mean etch rate of 12.0 $\mu\text{m/hr}$ for silicon as compared to 8.8 $\mu\text{m/hr}$ and 8.6 $\mu\text{m/hr}$ for negatively and neutrally charge electrets respectively. The one way Analysis Of Variance (ANOVA) of the silicon etch rates between the neutral

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1 INTRODUCTION

Electrets are materials with permanent “net” and “polarized” charges that reside on the surface or within the material [3]. Electrets are beneficial for providing a continuous electrostatic potential, over a range of fractional volts to several thousand volts, without the use of an external power supply. The electret provides an apparent potential at its surface, referred to as the effective surface voltage (ESV). Thin film electrets have produced some revolutionary devices such as the electret microphone and nonvolatile memory which remain functional for decades [4-6]. Traditionally, field effect transistor (FET) microphones, also known as electret condenser microphones (ECMs), are made with an electret consisting of a Mylar or Polytetrafluoroethylene (PTFE) [3, 7, 8]. Integration of surface mount electret microphones has been limited due to the inability of the polymer electret to maintain a charge throughout the surface mount reflow process which can be as high as 260°C. Inorganic electret materials, such as silicon oxide and silicon nitride have been shown to provide stable electret charge at elevated temperatures exceeding surface mount reflow process [2, 7-10]. Research has been conducted with these inorganic electret materials to integrate them in to MEMS microphones providing the benefits of system integration and charge stability [8, 9]. The mechanical properties, together with the established integration of silicon oxide and

silicon nitride films in MEMS platforms, makes these films an excellent choice for integrating electrets into MEMS devices [11]. The benefits of electrets as a permanent or semi-permanent electric field source has been realized in many other applications; Xerography [6, 12], dosimeters [13, 14], pressure sensors [10], energy harvesters [15], electro-active polymer (EAP) actuation [16, 17], and solar cells [18].

Thermally assisted poling, corona charging, and electron beam exposure are three methods frequently used to produce electret materials. Each method has its benefits and limitations; the best choice depends on the material to be charged, the application, and cost effectiveness. Corona charging and electron beam exposure are frequently used in microfabricated devices; corona charging is limited by the requirement of ion exchange, and both corona charging and electron beam exposure are limited by single polarity charging, and custom equipment to form the electret. Thermally assisted poling is the oldest method of electret formation. In this method, a mixture of carnauba wax and colophony (tree sap) is heated to its melting point while a high electric field is applied between two electrodes in contact with the mixture; the mixture is cooled to solidification under the electric field to produce the electret. Direct contact poling is rarely discussed as part of a MEMS based manufacturing process and has not been addressed for multilayer $\text{SiO}_2/\text{Si}_3\text{N}_4$ films. The new process presented does share some similarities to charge trap flash memory devices, with important differences in increased film thickness and the open faced charged film being unique to the electret produced. *The purpose of this study is to develop a PECVD $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ electret with a direct contact thermally*

assisted poling process that requires no ionic interface with the PECVD film surface as part of the charging process, can produce both positive and negative effective surface voltages with a single process polarization, and can be conducted with commercially available semiconductor processing equipment. There are three main aims to this study which will be investigated.

The primary aim is to develop a high temperature electret that can be programmed to provide a positive or negative effective surface voltage. A new method of direct contact electret activating a PECVD multilayer of SiO₂/Si₃N₄/SiO₂ is introduced with a study on optimizing the effective surface voltage of the film generated using a SUSS SB6+ anodic bonding system. The design of experiment consists of a 2³ full factorial analysis as a function of activation temperature, process time, and applied voltage.

A secondary aim of this study is to determine the activation energy of the electret film required to neutralize the effective surface voltage. The activation energy is determined by measuring the open circuit isothermal decay rate of the electret's effective surface voltage over time. The measurement is made at several elevated temperatures to determine the exponential decay rate of the charge. This data is fit to the Arrhenius function and the activation energy for positive and negative electrets is determined.

A tertiary aim is to explore the implementation of the electret as part of an electrochemical etch stop process. The electret acts as the "on wafer" bias required

for strong inversion and produces a depletion region for an etch stop, similar to the MIS etch stop presented by other groups [19]. The electrochemical etch stop makes use of a reverse bias at the dielectric-silicon interface as in a MOSFET and other MIS devices. Application of the electret in this type of etch stop targets a number of benefits including;

- no external power supply for the strong inversion of the MIS,
- no additional doping of the silicon, as required for a p-n junction etch stop,
- easy thermal neutralization of charge,
- and adjustable thickness control.

The PECVD film is treated at the die level in a direct contact activation process and test die are fabricated to determine if the electret is applicable to an etch stop in silicon. The electret is protected from direct etchant contact with the use of special etch cells and the etchant approaches the electret-silicon interface as the silicon etches. A number of timed etches are made and the progress of the etch depth is monitored over time to determine if the charge of the electret produces an effective depletion region to terminate the etch process. The effect of the electret's potential on the final etch rate of silicon is determined by the "Null Hypothesis" method. The "Null Hypothesis" for this set of experiments is that there is no statistical difference in the final etch rate between samples grouped by electret potential. An ANOVA is performed to determine if the null hypothesis can be rejected between any group of samples based on the charge of the electret.

2 BACKGROUND

The background is divided in two sections. The first half of the background will provide a review of the physical principles and forming techniques with historic context in the development of electrets. A brief review of electret applications is provided to give the reader an appreciation for the impact of electret technology. Several prominent researchers that have spent many decades developing a better understanding of electrets and have written detail review articles [6, 20-23]. Much of the background presented stems from these articles. The second half of the background covers the fundamentals of electrochemical etch stops in silicon with a focus on understanding how the effect of the electret may produce an electrochemical etch stop.

2.1 Introduction to Electrets

An electret is an insulating material characterized by the ability to maintain a charge and/or polarization while free from the equilibrium of applied external electric field [6]. Charges are fixed (or “frozen”), into the electret. The fixed charges are categorized as surface charges, space charges, and dipole charges, Figure 1. Surface charges are net charges that lay at the surface of the electret or at the

interface of material surfaces. Space charges lay within the material, although the charges may be concentrated in some regions and may not be homogeneously dispersed. Dipole charges arise when positive and negative charges are held together in small groupings but the small groupings align themselves in the greater whole of the material, producing a “net polarization” in the material. Multiple categories of charge may be involved in an electret and there can be multiple sources of charge to a category. As an example, both positive and negative charged ions may exist in the body of an electret as volume charges and induce polarization of dipoles as well. This would be modelled as two volume charges and one dipole charge. The discharge time duration (or lifetime) of each charging mechanism can vary drastically, from minutes to decades, depending on the nature of the charge, the material in which it resides, and the environmental conditions.

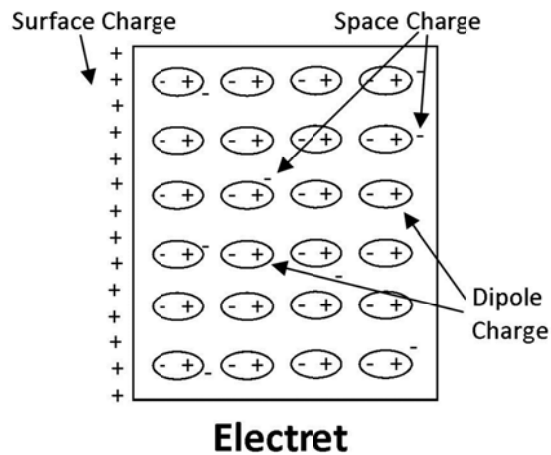


Figure 1. Electret material displaying fixed surface, volume, and polarized charges.

The observation of electret materials was documented by Stephen Gray in the early 1700's when he observed permanent surface charges of dielectric materials.

These early electrets were formed as dielectric materials consisting of wax and rosin developed net charges when cast and cooled in iron molds. Additional observations had been made by Heaviside in the late 1800's. Heaviside observed mobile charges within the insulating material migrating due to external applied potential and due to fixed polarization within a dielectric material. These mobile charges effectively mask the fixed charge from external surroundings. It was around 1920 that Mototaro Eguchi combined these two effects and was able to create thermoelectrets by applying external electric fields during the cooling and solidification process [6]. An appreciation for the complex nature of currents within the electret during charging and discharging developed in the early 1900's, as it became clearer that multiple current sources were acting, some caused by charge injection and others by ion mobility and bond breaking [24]. Properties of electrets on ionized gas and on the polarization of water have been understood for nearly a century [25].

Inorganic electrets including SiO_2 , Si_3N_4 , silicon oxynitride, and alumina have been well studied and they are popular choices in traditional semiconductor and MEMS applications [10, 26]. These inorganic electrets provide a number of charge trapping mechanisms; making use of dangling bonds, hydrogen defects, and bandgap interfaces. The wide bandgap of the outer silicon oxide films, in comparison to the interior silicon nitride film, provides a number of charge trapping opportunities. Composite multilayer inorganic electrets are favored over single

layers due to the improved charge retention over time and temperature [1, 2, 27-31].

2.2 Applications

Electrets are a fundamental part of the modern field effect transistor (FET) microphone used ubiquitously in many electronic devices today, such as phones. G. M. Sessler and J. E. West are often credited for the first commercially successful electret microphones based on their Mylar electroacoustic transducer invented in 1962 [32]. By their own admission commercially available wax electret microphones have been available since 1938 [33]. Electrets have been used in detecting ionizing radiation [34] and still have application in dosimeter applications [13, 35]. Recent developments include nonvolatile memory (NVM)[36, 37], vibrational energy harvesting [15], and improving the efficiency of solar cells [18].

The charge of an electret has an effect on the electric field of systems around it. As an example, the acoustic membrane of an electret microphone vibrates due to sound, acting as a vibrating variable capacitor that is dependent on the longitudinal pressure waves of the air. The electric field produced by the electret generates a change of potential between the variable capacitor plates. For a microphone integrated with a field effect transistor (FET), the sound dependent gate potential is transformed by the FET into a current output which provides a signal for additional amplification or transmission.

2.3 Insulator, Dielectric, Paraelectric, and Ferroelectric Properties

The characteristics and properties which define an electret often make it easy to confuse it with other material characteristics. To clarify the working definition of an electret, it is good to review some of the related characteristics of insulator materials. An ideal insulator does not conduct current; there is no charge transfer through the material. The ideal insulator is unaffected by external electric fields. Dielectric materials are affected by electric fields. The ideal dielectric produces an opposing polarizing electric field that is proportional to an active external electric field, Figure 2. The polarization of an ideal dielectric is linearly dependent on the magnitude of the external electric field applied.

Polarization comes in the form of electric, ionic, or dipole action from the material. These forms of polarization are dependent on many factors including, temperature, binding energy within material bonds, strength of electric field, photon interactions, drift and diffusivity, etc. Paraelectric materials exhibit a non-linear polarization as a function of the externally applied electric field, Figure 3. Not all polarization effects dissipate with the removal of the external electric field. Residual polarization is the result of newly trapped charges, ion migration, or a residual polarization of dipoles in the materials. Ferroelectric materials are considered electrets because they exhibit polarization in the absence of an external electric field [38]. The resulting polarizing hysteresis of ferroelectric material can be seen in Figure 4.

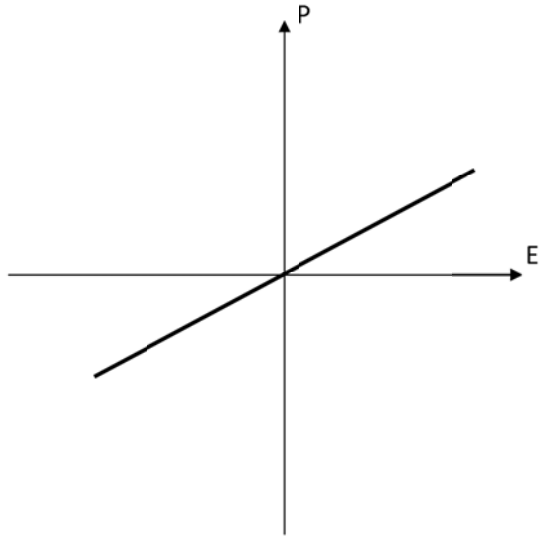


Figure 2. Dielectric materials exhibit a proportional polarizing electric field in response to an active external electric field.

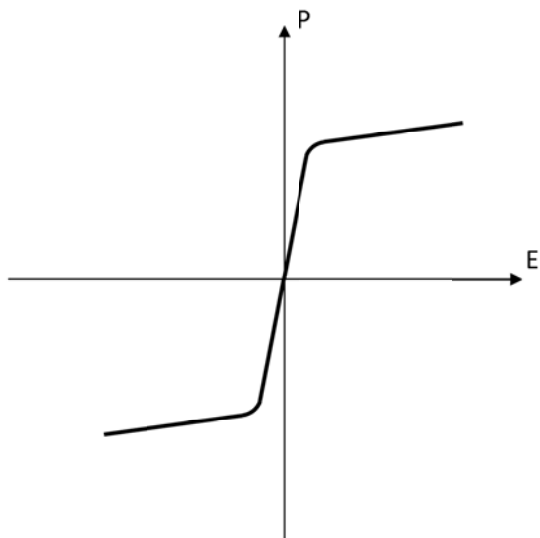


Figure 3. Paraelectric properties are exhibited by some dielectric materials as a nonlinear polarization as a function of an external electric field.

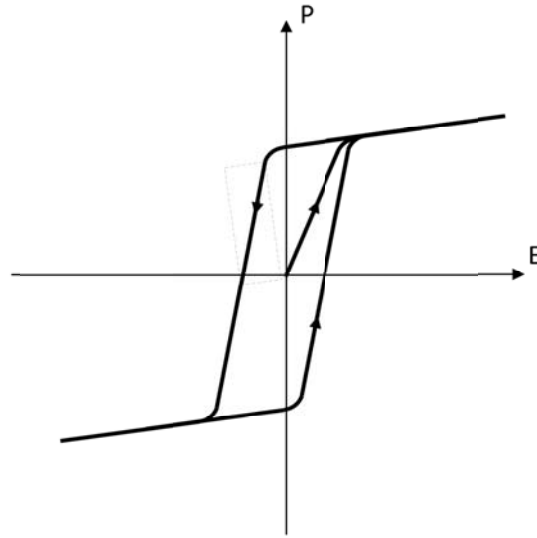


Figure 4. Ferroelectric properties are exhibited by some paraelectric materials with residual polarization without an external electric field.

Electrets exhibit polarization characteristics similar to those produced in a dielectric under biasing by an external electric field. Unlike the dielectric of a typical parallel plate capacitor, an electret can maintain its polarization field without it being induced by an external field. The remnant polarization, P_r , is the polarization remaining in the electret after the external electric field is removed. This remnant polarization is characteristic of a ferroelectric material due to dipoles [38]. The electret can also maintain “net” charges in different regions of the material; surface or space charge type. Remnant polarization and spontaneous polarization levels, P_s , are shown in Figure 5. The path of hysteresis shows the spontaneous polarization level as the polarization under the stress of the applied electric field. In the formation of an electret, this would be the polarization value during the activation

process. This hysteresis profile may be temperature dependent. A thermoelectret may follow a paraelectric polarization process at elevated temperatures resulting in a remnant polarization if cooled below the Curie-Weiss temperature before removal of the external electric field [38].

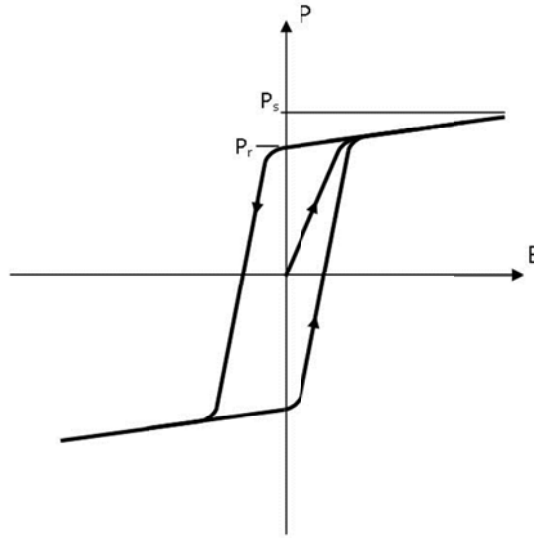


Figure 5. Polarization vs. electric field for a ferroelectric material. Spontaneous and remnant polarization levels are shown.

Figure 6, displays a categorization of insulators; all ferroelectric materials are paraelectric, all paraelectric materials are dielectric, and all dielectric materials are insulators. An electret can be formed in any of the regional definitions with the application surface charges, space charges, or dipoles. Some popular insulator materials are listed in each region of the Venn diagram. Each of the materials are categorized in the region they are commonly associated but this generalizations should be approached with caution. Materials often carry some of the

characteristics outside their typically defined region. Silicon nitride and silicon oxide are two such materials. These materials can be modified to operate under paraelectric and ferroelectric conditions with the introduction of traps, impurities, and composite construction [39]. All these conditions play an important part in SONOS and MNOS devices and they play a part in the composite electret as well.

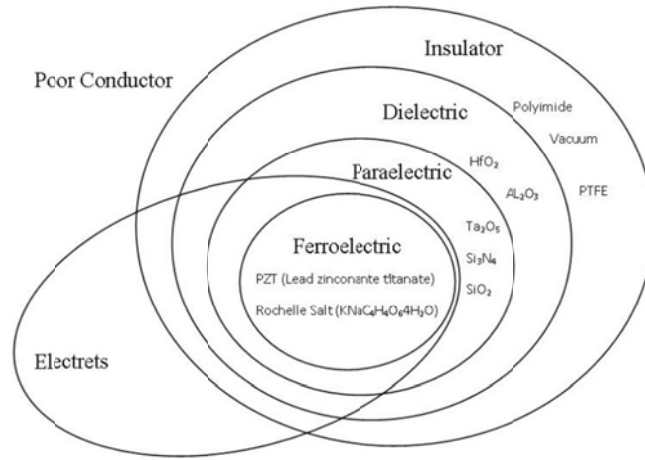


Figure 6. Venn diagram of insulator classification based on polarization behavior under the influence of an external electric field.

2.4 Comparisons of a thin film electret to a parallel plate capacitor

There are similarities and a shared background between electrets and dielectrics in capacitors that make it valuable to review the principles of a parallel plate capacitor before discussing the details of electret materials. Figure 7 (a) shows a capacitor consisting of two parallel plates made of conductive material in a vacuum. The parallel plate capacitor is “idealized” with the assumption that the two conductive plates have a large overlapping surface relative to the distance between

them. The surface charge density, σ_p , at the face of each plate varies proportionally with the potential, V , between the plates,

$$E = Vt = \frac{\sigma_p}{2\epsilon_0}, \quad \text{Equation 1}$$

where t is the distance between plates and ϵ_0 is the permittivity of free space.

An ideal capacitor contains identical charge densities on each plate, one net positive and the other net negative. While the capacitor can store this energy in a quasi-permanent time frame, the charges are mobile within each plate and will readily migrate to equalize in potential if given the opportunity. As the potential between the two conductive layers is increased, the charge (σ_p) on each conductive plate also increases. As the charge density on the conductive plate increases, the electric field between the two plates increases. As presented in the detail of Figure 7(b), the charge movement within the dielectric is limited and no charge is transferred from the dielectric to the conductive plates. Mobile charges and dipoles in the insulator respond in opposition to this electric field and reduce the net electric field between the two conductive plates when compared to an identical parallel plate configuration without the dielectric. The electric field, E , between the parallel conductive plates is given by,

$$E = \frac{\sigma_p}{2\epsilon_0\epsilon_r}, \quad \text{Equation 2}$$

where ϵ_r is the relative permittivity of the dielectric between the conductive plates and ϵ_0 is the permittivity of free space.

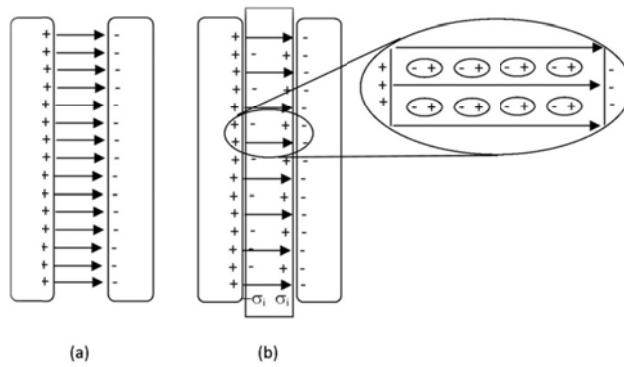


Figure 7. (a) Parallel plate capacitor with free space permittivity. (b) Parallel plate capacitor with dielectric material.

Figure 8(a) provides a representation of the dielectrics polarization in response to an external electric field applied across the conductive plates. Once the external electric field from the conductive plates is removed from the dielectric, the polarization of the ideal dielectric returns to a state of zero polarity because the external electric field forces are no longer acting on the semi-mobile charges within the dielectric. Figure 8(b) provides a representation of the dielectric's polarization response when there is no external electric field applied; this is not the case for an electret.

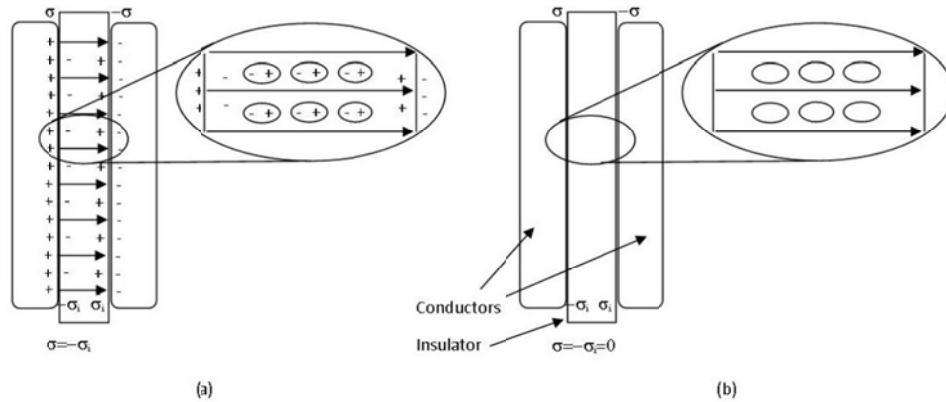


Figure 8. A dielectric insulator is sandwiched between two metal layers. (a) Opposing charges on conductors generate electric fields (arrows: positive to negative charges) and produce an opposite polarization by charge migration. (b) The removal of an external electric field on the dielectric reduces the charge polarization in the dielectric to zero.

At first glance, the response to an applied external electric field in the lower detail of Figure 9(a) looks typical for a dielectric in a parallel plate capacitor. The upper detail to Figure 9(a) shows a new concept; that surface or space charges developed in the insulator are similar in polarity to the conductors. This type of space charge usually develops as charges “leak” from the conductor into the insulator. The charge leakage may also occur in a typical dielectric, but the polarity of the space charge is significant when looking at Figure 9(b). In Figure 9(b), the removal of the conductors is equivalent to the removal of the external electric field on the insulator. In this case, the insulator is left with a residual charge and polarization; this ferroelectric characteristic has transformed the insulator to an electret.

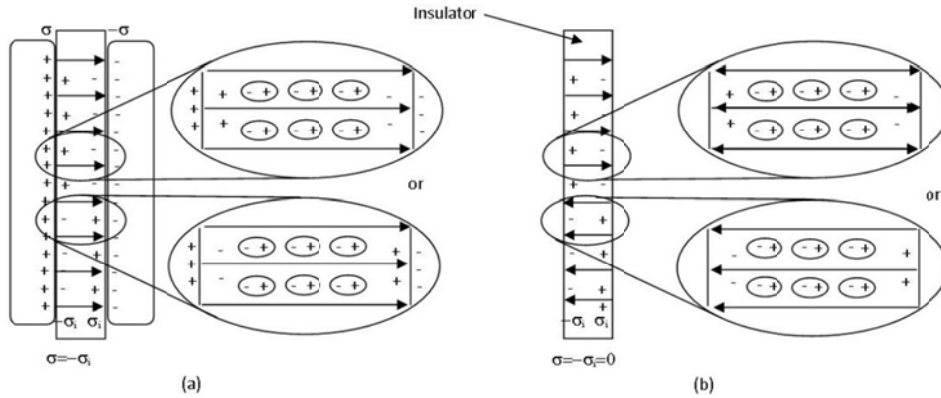


Figure 9. A ferroelectric insulator is sandwiched between two metal layers. (a) Opposing charges on conductors generate electric fields (arrows: positive to negative charges) and produce a polarization by charge migration; upper detail leaking charge, lower detail opposing charge. (b) The removal of an external electric field on the insulator does not negate the charge polarization.

2.5 Electric Displacement Field

A review of electric displacement, D , is needed to understand the relationship between charges in a dielectric and the forces that the charges can produce externally. Basic dielectric materials have a linear electric field induced polarization, P , as a function of the electric field, E . The polarization can be calculated as a function of permittivity of free space, ϵ_0 ; relative permittivity of the material, ϵ_r ; and susceptibility, X , as shown in

$$\vec{P} = (\epsilon_r - 1)\epsilon_0\vec{E} = X\epsilon_0\vec{E} \quad \text{Equation 3}$$

and results in an electric displacement, $D_{\text{dielectric}}$, for the basic dielectric

$$\vec{D}_{\text{dielectric}} = \epsilon_0 \vec{E} + \vec{P} = \epsilon_r \epsilon_0 \vec{E}. \quad \text{Equation 4}$$

The electric displacement provides a complete description of the resulting force due to the electric field and polarization [40]. It is not required that the relative permittivity of the material, ϵ_r , be constant. The relative permittivity of paraelectric materials typically decreases as the electric field increases, as presented earlier in Figure 3. The displacement field becomes more interesting with ferroelectric materials where residual polarization exists without any electric field. In this case, the polarization of a ferroelectric material can be treated as a constant and for the rest of this discussion will be considered as a component of electrets, referred to as P_{electret} . Electrets may also have space charges and surface charges. In device design and many practical applications these real charges are lumped together as an effective surface charge, σ_{electret} . The summation of the electric field induced electric displacement (Equation 4), the permanent polarization, and the effective surface charge represent the complete electric displacement field

$$\vec{D}_{\text{electret}} = \epsilon_r \epsilon_0 \vec{E} + \vec{\sigma}_{\text{electret}} + \vec{P}_{\text{electret}}. \quad \text{Equation 5}$$

The general model presented in Figure 10 is useful in understanding how the charge of a thin film electret affects its surroundings. The effects of a moving conductive plate, effective surface charge measurements, and the electret's effect on

semiconductor interfaces will all be addressed with this fundamental model. The basic outline follows from Chapter 2 in Sessler's "Electrets: Topics in Applied Physics" [6]. The model assumes ideal infinite planes and the analysis can be simplified to a 1-D model. The layers consist of a bilayer dielectric material backed with a metal electrode. The dielectric layer is modeled as an electret and is separated from the upper electrode by an air gap. The voltage, V_0 , across the free and backing electrode provide for applied potential or measured potential; current may also be measured between electrodes as the configuration changes states based on the application of boundary conditions.

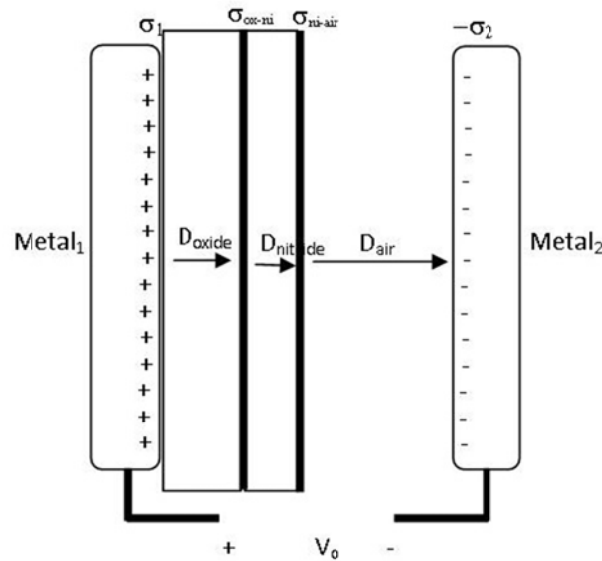


Figure 10. A simple model consisting of a conductive backed multilayer electret of silicon oxide and silicon nitride for modeling effective surface voltage and microphone operational principles.

Kirchhoff's second law, with regard to charge, provides

$$t_{oxide} \frac{D_{oxide}}{\epsilon_{oxide}} + t_{nitride} \frac{D_{nitride}}{\epsilon_{nitride}} + t_{air} \frac{D_{air}}{\epsilon_{air}} = V_o \quad \text{Equation 6}$$

The displacement fields of the oxide layer and air layer are defined by the surface charge density of their respective metal electrodes

$$D_{oxide} = \sigma_1 \quad \text{Equation 7}$$

$$D_{air} = \sigma_2 . \quad \text{Equation 8}$$

Any change in the displacement field intensity is modeled to be due to a fixed surface charge density between layers

$$-D_{oxide} + D_{nitride} = \sigma_{ox-ni} \quad \text{Equation 9}$$

$$-D_{nitride} + D_{air} = \sigma_{ni-air} . \quad \text{Equation 10}$$

In the “non-electret” case, there are no fixed charges in the dielectrics or interfaces, $\sigma_{ox-ni} = \sigma_{ni-air} = 0$. The displacement field in each region of film is equal, $D_{oxide} = D_{nitride} = D_{air}$, regardless of any applied voltage, V_o . With no charges located at the oxide-nitride interface and/or the nitride-air interface, $\sigma_1 + \sigma_2 + \sigma_{ox-ni} + \sigma_{ni-air} = 0$. The charge on metal₁ and metal₂ are oppositely charged and equal in magnitude, $\sigma_1 + \sigma_2 = 0$.

With devices that make use of a change in air gap, t_{air} , differentiation of Equation 6 is used determine how the effective charge density on the simple metal electrode effected by a change in the air gap, t_{air} .

$$\frac{d\sigma_2}{dt_{air}} = \frac{-(V_0 + \frac{\sigma_{ox-ni}t_{oxide}}{\epsilon_{oxide}})}{\epsilon_{air}(\frac{t_{oxide}}{\epsilon_{oxide}} + \frac{t_{nitride}}{\epsilon_{nitride}} + \frac{t_{air}}{\epsilon_{air}})^2} \quad \text{Equation 11}$$

results in a transduction of air gap thickness, t_{air} , to voltage, V_0 . The attractive force, F , per unit area, A , or electrostatic pressure P , between the plates is

$$\frac{F}{A} = P = \frac{\sigma_2^2}{2\epsilon_{air}}. \quad \text{Equation 12}$$

2.6 Effective Surface Voltage Electret Measurement

The effective surface voltage (ESV) of the electret film is measured using noncontact methods. The most commonly used measurement system is null seeking feedback vibrating capacitor field meter, Figure 11 [41] [42]. The meter detects the effective surface voltage by elevating the potential of the external case of the probe until it cancels any external field detected by the internal resonating capacitor which is exposed to an external field through a small aperture. Effective surface voltage (ESV) measurements can be modelled with a new set of boundary conditions for the same model presented in Figure 10. In the case that there are trapped charges at the oxide-nitride interface, $\sigma_{ox-ni} \neq 0 = -\sigma_1$, and $\sigma_{ni-air} = 0$.

Here metal₂ acts as the free electrode (electrostatic meter probe) and its potential is adjusted, using feedback control circuitry, to a point that $D_{air} = 0$ and $D_{ni} = 0$, which means that $\sigma_2 = 0$ and $\sigma_{ox-ni} = -\sigma_1$. Equation 6 simplifies to

$$t_{oxide} \frac{D_{ox-ni}}{\epsilon_{oxide}} = V_o \quad \text{Equation 13}$$

where the voltage, in Figure 11, is the effective surface voltage of the electret film as measured by the electrostatic voltmeter. As an example, with a permittivity of $3.45 \times 10^{-11} \text{ C}/(\text{V}\cdot\text{M})$ and a silicon oxide thickness of 1650 nm, an interface charge of 4.71 mC/m² at the blocking oxide-silicon nitride interface will produce an effective surface voltage of 225V.

Isothermal potential decay (ITPD) data is collected by taking ESV measurements as a function of time at a specified temperature [2]. The exponential decay of the ESV at different elevated temperatures allows for extrapolation of the ESV at room temperature (or the designed operating temperature) so that the system making use of the electret film can determine its useful lifetime. It is important to recognize that multiple slopes may emerge on the Arrhenius plot of the lifetime coefficient as a function of temperature. This can be due to increases of thermal energy required to initiate charge migration in electron/hole trapping mechanisms, dipole relaxation times, and ion migration [43]. Protective coatings promoting hydrophobic behavior of the electret may deteriorate at elevated temperatures and present it in ITPD data above, the decomposition temperature of the protective coating.

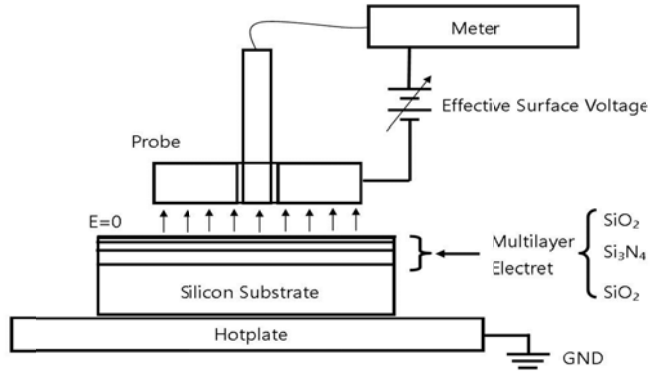


Figure 11. Diagram of null seeking feedback vibrating capacitor field meter with electret and substrate.

The measurement of the electrets effective surface voltage may require special consideration when the electret is backed by a semiconductor. The bulk of the semiconductor is grounded but there is band bending in the semiconductor to take in to consideration. Viewing the effective surface voltage as the gate potential of a MIS capacitor, the total voltage measured as the effective surface voltage V_{esv} , is the potential across the electret $V_{dielectric}$, and the potential due to band bending in silicon is ϕ_s , shown in Figure 12 and given by

$$V_{esv} = V_{dielectric} + \phi_s. \quad \text{Equation 14}$$

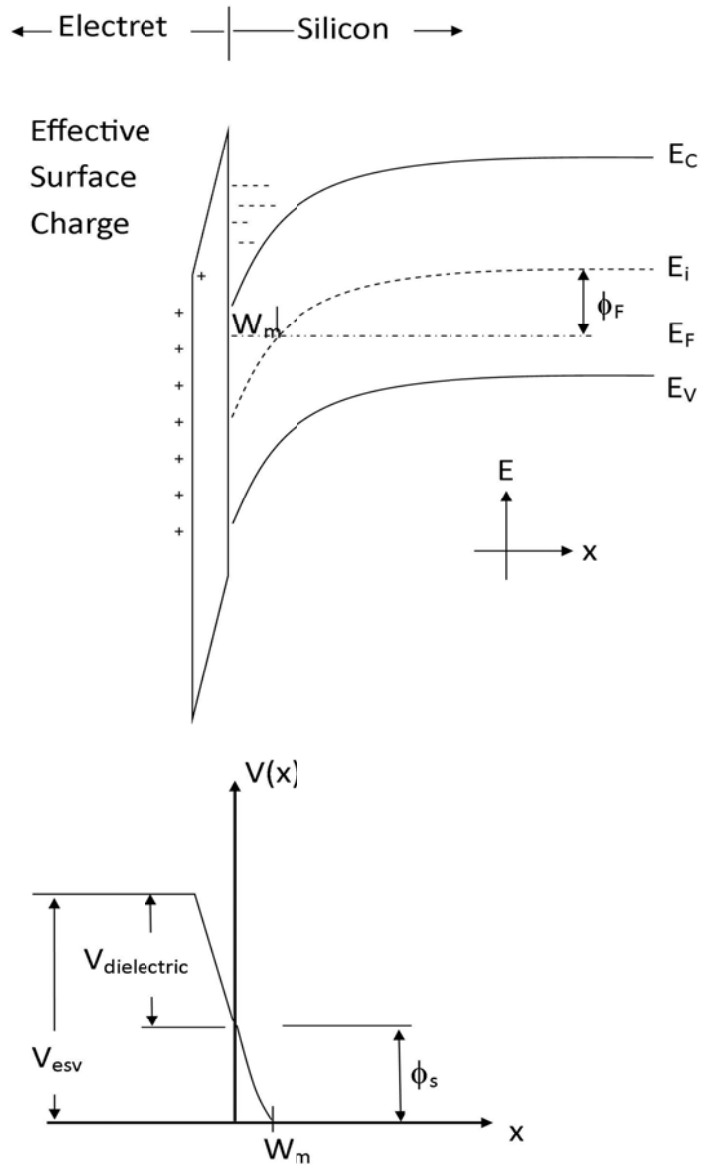


Figure 12. Insulator-silicon band bending due to electret bias modelled as an effective surface charge.

2.7 Electret Formation

Thermally assisted poling, corona charging, and electron beam implant are three frequently used to produce electret materials. Each method has its benefits and limitations. The best choice depends on many factors including the material to be charged, the application, and cost.

2.7.1 Thermally Assisted Poling

Thermally assisted poling is the original method used in generating an electret film [6]. Thermally assisted poling typically takes place throughout the bulk of the material as the sample is heated near or past a critical transition temperature of the material while an external potential is applied across the sample. Original experiments were with blends of carnauba wax and colophony (tree sap) that were brought down from melting temperatures to solidify under the application of an external electric field. Likewise, thermally assisted activation of PTFE at temperatures near its glass transition temperature was found to improve the quality of electret formation both in charge density and increase its lifetime temperature endurance [6]. Ferroelectric dipole electrets rely on polarization near or over their Curie temperature. Electrets formed from multilayer dielectrics such as $\text{SiO}_2/\text{Si}_3\text{N}_4$ rely on thermal assistance to increase the Poole Frenkel conduction and thermal charge injection required to create deep trapping layers and fill them with charges.

2.7.2 Corona Charging

Corona charging is inexpensive to implement and is easy to implement for large surface areas. Without heating the charge material, its charging method is limited to surface charging and ferroelectric polarization [22]. Heating the electret during corona charging can assist the electret activation process; thermally assisted activation with the corona field applying the potential to the electret surface provides additional opportunities with volume charging and a broader range of dipole charging effects [22].

Corona charging is a frequently used method that makes use of ionized gases; the process can run at atmospheric pressures. In the case of corona charging, the ions produced from ionized gas, which is often room air, are propelled to the surface of the electret activated material. There are a number of reactions caused by corona charging that can complete the electret activation. Ions can react with the surface of the film and complete a covalent bond which results in a net charge at the surface. The ions can also accumulate at the surface without bonding and act as a flexible charge distribution that applies a potential through the dielectric film [2]. During heating this ion induced field applies the potential required for thermally assisted poling. As a third process, the ions may not bond with the surface but may diffuse into the surface of the electret film with a resulting net ionization charge distribution just below the surface. Corona activation of PTFE is transformed from a

surface charge effect to space charge activation with thermally assisted poling temperatures approaching the glass transition temperature of PTFE [6].

Continuous rolled polymer sheets and xerography systems typically use wire discharge systems to promote even charging along the width of the sheet. Corona charging for silicon based MEMS devices is traditionally done at wafer level with a point discharge and grid, as shown in Figure 13, although there have been recent developments with in situ device level charging using built in microelectrodes [44].

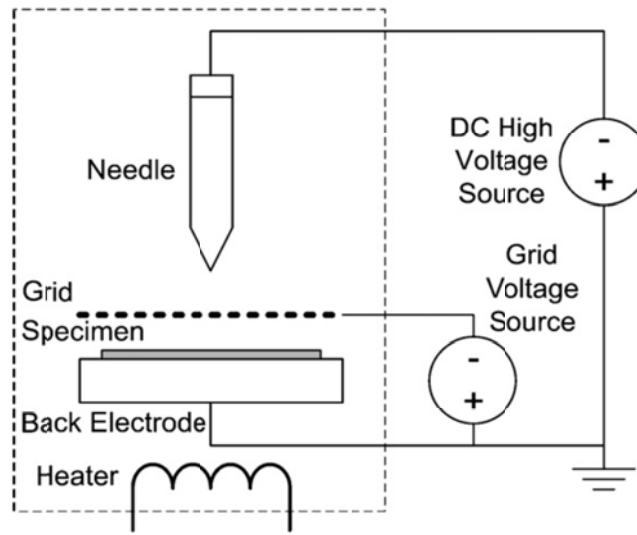


Figure 13. Corona charging schematic with heat assistance [44].

Electron beam charging of the dielectric typically requires processing in a vacuum. Sources are available which can provide large surface area coverage as well as localized patterning. Electron beam charging provides volume charging to the electret and can also provide surface and polarization charging with thermal assistance. Electron beam charging can produce the obvious negative charged

regions in the insulator. Electron beam charging can also produce positively charged regions due to the secondary emission and scattering of electrons within the substrate; secondary electrons within the substrate can be knocked out of the substrate leaving a net positive region [45]. Thermally assisted electron beam charging can take advantage of the newly created traps generated by the electron damage [6, 22].

2.7.3 Electron Beam Implant

Back-light Thyratron (BLT) sources make use of the Townsend avalanching ionization of a noble gas, such as hydrogen, under vacuum. The free electrons are propelled by the high electric field to implant into the electret surface[46]. Electron implanting can produce net positive or negative electret films depending on the kinetic energy of the electrons. Low energy electrons will embed themselves just below the surface of the film. As the implant energy is increase the mean depth of the implant increased. With high energy, the electrons can actually cause secondary electrons to be scattered out of the film, resulting in a positive charge because of the loss of negative charges [45].

2.8 Charge Traps in SiO₂ and Si₃N₄

Silicon oxide and/or silicon nitride have several advantages as electret material candidates. These inorganic electrets are noted for withstanding high temperature environments while maintaining their charge [7]. Inorganic electrets composed of

silicon nitride or silicon oxide can have a thermally stimulated discharge temperature as high as 500°C where traditional fluorinated electrets like PTFE have a lower thermally stimulated discharge temperature in the range of 200°C to 250°C [22]. Silicon nitride and silicon oxide are also compatible with microelectronic and microfabrication processing. This is particularly advantageous given the microfabrication capability of getting this fixed charge to interact in a controlled manner over such small dimensions. Effective surface voltages of -300 V have been reported for SiO₂/Si₃N₄ electrets [26].

Charge trapping is an important part of nonvolatile memory (NVM). A multilayer film of SiO₂/Si₃N₄/SiO₂ on a silicon wafer is used to construct the nonvolatile gate used in silicon-oxide-nitride-oxide-silicon (SONOS) memory [5, 47]. The multilayer properties of a SiO₂/Si₃N₄ film on silicon are considered as wide bandgap materials. Multilayer dielectrics provide additional charge trapping opportunities with the collection of interface trapped charges, and setting barriers for fixed trap charges and mobile ion charges. The charge trapping effects have been shown to survive 15 hrs of elevated temperature at 150°C [47]. The multilayer film traps charges in the silicon nitride which hold the state of the gate memory [48]. The high hydrogen content within the deposited silicon nitride film provides for Si-H, dangling bonds and Si-Si states that act as amphoteric traps for trapping charges [49]. Elevated temperature studies on SONOS memory devices have shown that elevated temperatures of 175°C are detrimental to excess electron charge

states due to thermal electron emission but the elevated temperature has no effect on hole charge decay rate [50].

2.9 Studies of SiO₂/Si₃N₄ Multilayer Electret Activation

Research has been done on electret formation of a PECVD SiO₂/Si₃N₄ double layer by corona charging [2]. Temperature has played a role in the study but the temperature range has been limited in range from room temperature to 80°C. Amajadi et al. [51] noted that single layers of corona charged oxide or nitride did not maintain the electret charge for a period of more than a few days without coating with HMDS. Silicon nitride corona charged and HMDS coated was also shown to be very susceptible to high humidity environments. Amjadi and Sessler 1997 [52], studied a single layer of atmospheric pressure chemical vapor deposition Si₃N₄ charged in a corona field at room temperature and showed that the peak current of the open circuit thermally stimulated current occurred at about 410°C, Figure 14.

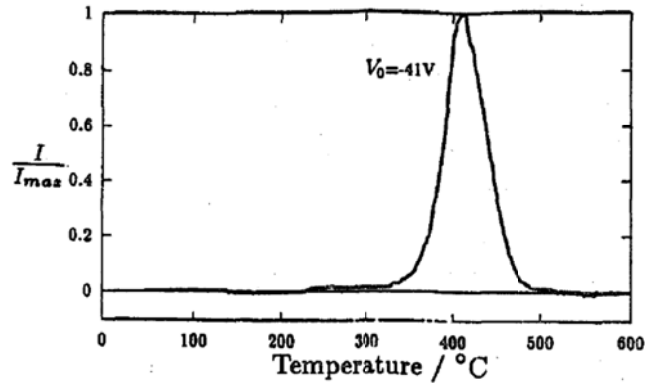


Figure 14. APCVD Si₃N₄ open circuit thermally stimulated decay [52].

Leonov provides details on an effective procedure for pre and post annealing in conjunction with corona charging of the electret. The results show that pretreatment of the LPCVD generated silicon nitride with thermal oxide layers benefit from a dehydration bake when it comes to the decay life of the electret charge. The results also show that a post processing anneal of around 250°C initially causes a rapid field loss; it has also be documented by Leonov that a heat pretreatment at 450°C produced the most durably held field and with only 1-2% charge loss as compared to a typical 20% loss by process with lower temperature pretreatments of the film [28]. The range of temperature ranges used in pre and post treatments show that multiple charge trapping mechanisms are involved. Surface treatment modifications to silicon nitrides and silicon oxides have shown drastic differences in the lifetimes of the electret charge. The lateral surface conduction on a silicon oxide surface, which normally makes it a poor electret candidate, is easily modified with a coating of HMDS to minimize surface conduction resulting in an electret with a lifetime constant of over 400 years [7]. This coating process is performed to remove water vapor and prevent reabsorption of the water in to and on the surface of the film since it has been well documented that water and humidity cause neutralization of the effective surface voltage as polarized water molecules adsorb to the electret and mask the charge [11]. Upon deposition, the HMDS reacts to form a trimethylsilyl (TMS) monolayer on the multilayer PECVD electret [7, 53]. The TMS monolayer makes the multilayer surface hydrophobic and prevents the deleterious effects of humidity from neutralizing the electret.

Voorthuyzen et al. used a unique form of thermally stimulated decay for determining the thermal energy required to overcome the trapped charges in corona charged silicon oxide electret [54]. Here the samples were subjected to elevated temperatures over 20 minute intervals, cooled, evaluated with a Monroe electrostatic voltmeter, and then again heated to a higher temperature than the previous 20 minute interval, Figure 15. A notable thermal decay starts to appear at temperatures over 275°C.

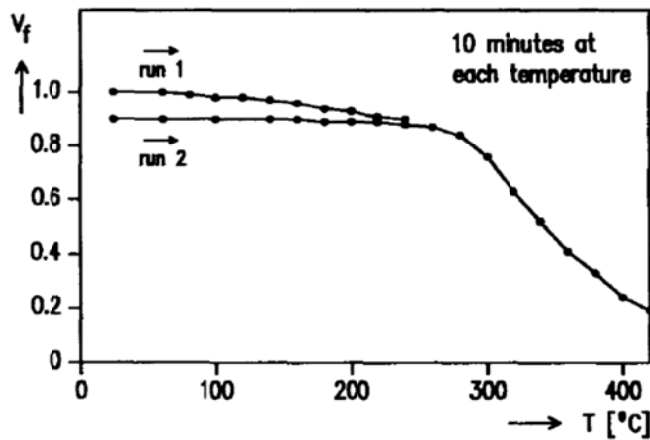


Figure 15. Normalized effective surface voltage TSD of corona charged silicon oxide electret [54].

2.10 Charge Trapping in SiO₂, Si₃N₄, and Multilayer Electrets

The conductivity of silicon nitride plays an important part in the electret properties of an oxide-nitride-oxide (ONO) multilayer. Conductivity of the silicon nitride can be increased by forming a silicon rich nitride (SRN) and allows a larger portion of the trapped charge to migrate to the oxide/nitride interfaces during

poling [55], Figure 16. LPCVD has been used as a method for producing SRN films. LPCVD silicon nitride films are generated in a temperature range of 700-900°C from dichlorosilane and ammonia gas, although the excess ammonia gas concentration makes it relatively easy to produce stoichiometric Si₃N₄. Hydrogen is a component to LPCVD and PECVD nitrides and oxides due to the use of silane and ammonia gases. LPCVD silicon nitride typically contains a lower hydrogen content versus PECVD silicon nitride, 8% vs 25% respectively. LPCVD silicon nitride can be a good barrier to hydrogen diffusion and has resistivity on the order of 10¹⁶ ohm*cm. In contrast, the PECVD silicon nitride has a high hydrogen content and the resistivity is on the order of 10⁵ to 10²¹ ohm*cm [56]. The hydrogen content is considered a liability to producing durable insulators with high breakdown voltages but the silicon-hydrogen and nitrogen-hydrogen bonds produce defects which can become active charge traps when the hydrogen is released during heating and under large electric fields. The electron trap density within the bulk of silicon nitride increases as the temperature decreases from 150°C to room temperature. As this total trap density increases with lowering temperature, the interface electron trapping at the Si₃N₄/SiO₂ interface decreases [55]. Ultrathin films and films over 10nm take into consideration Trap Assisted Tunneling (TAT) [57, 58].

Frenkel Poole (FP) conduction is considered the primary source of charge transfer with fields applied across SiO₂ and Si₃N₄ films over 10 nm [5, 59]. The Frenkel Poole effect occurs under high electric fields, starting at 2-5 MV/cm for silicon nitride, and is due to electrons or holes migrating from one shallow trap site

to the next. This “hopping” process is a function of temperature as the charge temporarily gains enough thermal energy to break free of the trap site. Ultra-thin films ,less than 10 nm, and multilayer dielectric stacks with ultrathin films such as MNOS and SONOS devices rely on a combination of FP conduction with tunneling, usually Fowler Nordheim (FN), Figure 16. The charges injected through Fowler Nordheim tunneling migrate by Frenkel Poole conduction and build up at the opposing silicon nitride- silicon oxide interface.

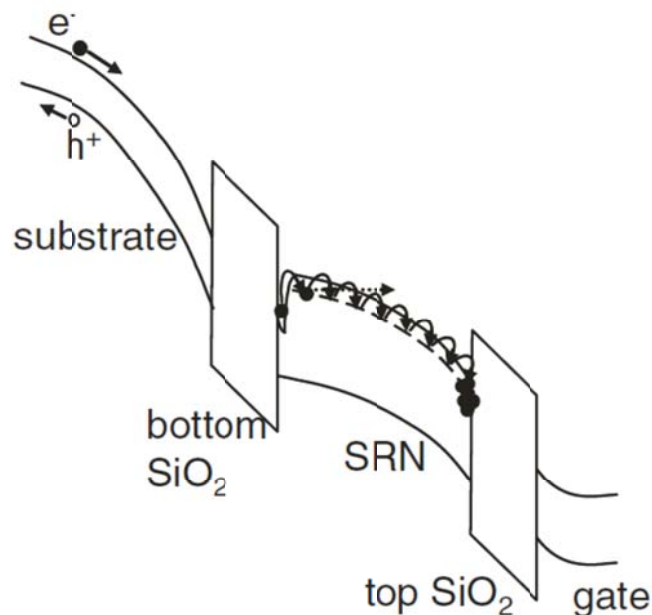


Figure 16. SONOS band diagram with Poole Frenkel conduction in silicon nitride.

Source: [55]

The silicon dangling bonds are amphoteric due to being relatively well centered in the band gap of the silicon nitride regardless of the stoichiometry of nitrogen to silicon, Figure 17. The number of silicon dangling bonds dominate nitrogen

dangling bonds with and without post deposition heat treatments of 600°C but silicon dangling bonds are reduced by the heat treatment while nitrogen dangling bonds remain unchanged [60]. Nitrogen dangling bonds only become a trap consideration as the ratio of nitrogen to silicon is increased in the CVD process. The presence of the nitride dangling bonds are seen near the valence band, inside the silicon nitride band gap, as the band gap widens with an increase in the nitrogen to silicon ratio, Figure 17.

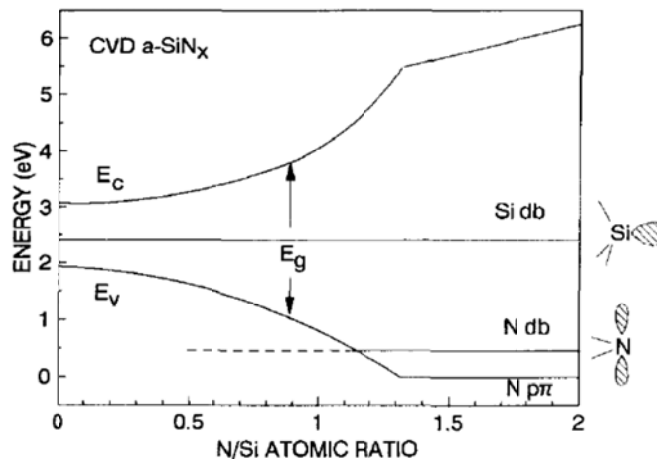


Figure 17. Nitrogen to silicon ratio effect on silicon nitride band gap is shown with silicon dangling bond and nitrogen dangling bond levels [60].

Hydrogen diffusion and the role of hydrogen in bonding plays a factor in the electret charge created at the $\text{SiO}_2/\text{Si}_3\text{N}_4$ interface [61]. Amphoteric traps, due to dangling bonds, are responsible for the charge trapping in silicon nitride [50, 62-64]. Hydrogen has been shown to fill the traps of the dangling bonds of silicon and nitrogen in the silicon nitride layer. High temperature inert annealing can free those

hydrogen atoms and increase the number of dangling bonds while annealing in hydrogen can decrease the dangling bonds [4, 5].

Charge traps can be generated in SiO_2 under thermally assisted electric fields of 1.5 MV/cm [65, 66]. The hot carrier electrons injected into the oxide are capable of releasing hydrogen from defect locations near the anode surface when the electron energy is 2eV or greater. These positive charged hydrogen ions can migrate to cathode region of the oxide creating interface states near the cathode for electron traps, Figure 18. This process is considered independent of oxide thickness for films over 10 nm. This process a good candidate for each of the dielectric layers in our PECVD multilayer film. The effect of hydrogen on the performance of NVM is well documented and particularly a concern in hydrogen rich PECVD films [49, 61, 67]. Higher energy hot carrier electrons can produce inelastic scattering capable of producing secondary electron-hole pairs available to fill deep trap locations [68]. Annealing samples in the temperature range of 200°C to 300°C releases the hydrogen from Si and N bonds in silicon nitride leaving them as susceptible trapping locations [5].

Impact ionization is significant when field strengths are greater than 7 MV/cm in SiO_2 . At these high electric fields, the electron energy distribution broadens and the energetic tail of hot-electron energy is significant enough to cross the silicon-oxide Schottky barrier height. Using deep-level transient spectroscopy (DLTS), the trap levels have been measured for ONO layers [69]. ONO has hole traps that are 0.5-

0.64 eV above the valance band of silicon and has electron traps in two ranges 0.25-0.45 eV and 0.47 – 0.63 eV below the conduction band of silicon.

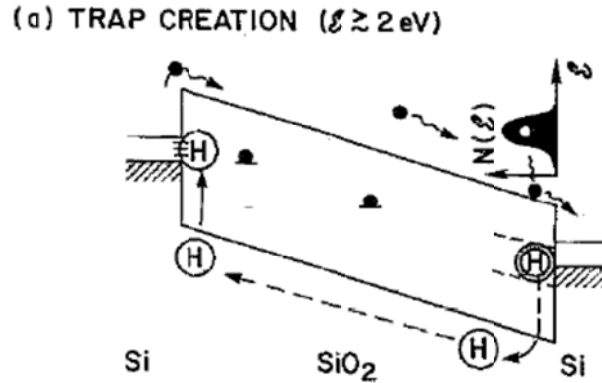


Figure 18. Hot carrier electron injection in to silicon dioxide and hydrogen release [68].

2.11 Analysis Techniques of Electrets

The apparent charges of an electret can be in the form of surface charges, space charges, and or charge dipoles. Multiple charging principles can be involved and the lifetime rates of each type of charging source can be drastically different in the same material. As an example, charges injected from direct contact sources may last for a few days, while the polarization and other heterocharge sources will last months and years [6]. A range of temperature based lifetime measurements, surface voltages, open or closed circuit current measurements, and frequency responses provide several opportunities for evaluation of the electret's operation.

A number of complementary measurement techniques make it possible to understand the inner workings of the electret's charge profile and properties. A review of additional measurement techniques can be reviewed in [6, 38]. The electric field originating from an electret is measured by controlling the position of a grounding plane with a vibrating capacitor field meter to an effective surface voltage (ESV) to the electret. Measurements at elevated temperatures can be used to provide isothermal potential decay measurements. These two methods will be discussed in greater detail in the following section.

Thermally stimulated discharge current (TSDC) or thermally stimulated current (TSC) is measured from the electret as charges and/or dipoles relax and discharged as a function of temperature. Charges released as a function temperature provide an estimate for the energy level of the trapped charge. Thermally stimulated discharge (TSD) enables the identification of the relaxation mechanisms of the electret as a function temperature [70]. Two common configurations are the air-gap TSD and the direct contact TSD. In the air-gap TSD configuration the electret is between two electrodes but one electrode is not in direct contact, limiting transfer of charge to or from the electret [38]. The direct contact TSD configuration is, just as described in its name, with the electret sandwiched between electrodes. The use of both methods on a material helps to provide a complete picture of the charge and polarization responsible for the electret characteristics. Monitoring the current of the air-gap configured TSD, due to the discharge of the electret as it is heating, provides a temperature depended profile of the dipole relaxation temperatures.

Monitoring the current of the direct contact TSD configuration while the electret is heating, allows for both net charge and dipole relaxation currents to be monitored simultaneously. Using both permits separation of the current data due to each the charge migration and the dipole relaxation.

Deep-level transient spectroscopy (DLTS) or transient capacitance spectroscopy (TCS) monitors the variation in capacitance as a gradual change in temperature is made [38]. There are many variations to this measurement technique, in semiconductor junctions the space charge region is pulsed with a forward biased so that trap locations can be refilled. The capacitance is monitored over time to look at the emptying of these traps at various temperatures.

The pulsed electro-acoustic (PEA) method uses two direct contact electrodes and an applied electrical pulse to apply a force to the trapped charges of the electret. This induces a displacement in the electret which propagates to a piezoelectric crystal mounted on one side of the electret. The piezoelectric crystal in turn produces an electric potential which can be monitored. The time delay between the input signal and output of the piezo crystal provides information on the physical depth of the charges within the electret and the intensity of the output relative to the input provides information on the effective charge density [38].

It is possible to tell what part of the electrets electric field is due to polarization by looking at the difference in the films permittivity before and after electret activation. It depends on the magnitude of the field through the material and the

frequency of the electric field. Polarization of a ferroelectric material can be measured with a Sawyer-Tower circuit to produce the polarization vs electric field profile.

A Kelvin probe is used in a manner similar to the electrostatic voltmeter to measure surface photovoltage (SPV). This noncontact method looks at the effective surface voltage of a semiconductor such as silicon to evaluate the charge build up in the space charge region (SCR) with the sample cycling between light and no light exposure. From these measurements, the minority carrier diffusion length can be determined in a noncontact method. This method is a standard practice in the CMOS industry for measuring defect densities in the 10^9 - 10^{11} cm^{-3} range [39].

2.12 Concepts in Modeling Temperature Dependent Exponential Decay

The objective of this section is to introduce the concepts of modeling exponential decay and then implement those concepts in defining the characteristics of the effective surface voltage decay for the PECVD oxide/nitride/oxide multilayer electret. The temperature dependent decay of the electret is used to; first, extrapolate the expected decay rate of the electret at room temperature and common operating temperatures; and second, investigate the energy level of charge trapping in the material.

The effective surface voltage is a result of trapped charges and polarization within the dielectric film stack film and silicon substrate as presented earlier in

section 2.10 - "Charge Trapping in SiO₂, Si₃N₄, and Multilayer Electrets". Diffusion based migration of charge would dominate if no activation energy is required. The activation energy required to release charge traps is provided thermally. The trap sites are due to bond defects and band interfaces at junctions between dielectric layers and the silicon wafer. The charges in these filled trap locations have a greater probability, at higher temperatures, of having sufficient energy to move to a higher energy state where they can either drift or diffuse. Externally applied electric fields and internal electric fields provide the electric field for drift.

First order exponential decay is a common occurrence in nature. It stems from a quantity, such as a concentration, changing with time in constant proportion to that quantity. The equation

$$\frac{dN(t)}{dt} = -\lambda N(t) \quad \text{Equation 15}$$

represents this behavior where N(t) is the concentration at any given point of time, t, where λ is the exponential decay constant. Given the initial condition of a concentration N_o at time t=0, the exponentially decaying quantity is determined by integration of Equation 15, resulting in

$$N(t) = N_o e^{-\lambda t}. \quad \text{Equation 16}$$

where N_0 is the initial concentration. The mean lifetime is the average period of time for the initial concentration to react. It can be calculated from the exponential decay formula, Equation 16. The mean lifetime (τ) is determined by integration of the time weighted decay

$$\tau \text{ or } \langle t \rangle = \frac{\int_0^{\infty} t N_0 e^{-\lambda t} dt}{\int_0^{\infty} N_0 e^{-\lambda t} dt}. \quad \text{Equation 17}$$

The result is that the mean lifetime is the inverse of the exponential decay quantity $\tau=1/\lambda$. At time, $t=\tau$, the concentration is

$$N(\tau) = \frac{N_0}{e}. \quad \text{Equation 18}$$

Mean lifetime is easy to extract from curve fits and but it is usually difficult to visualize e^{-1} of the initial concentration. For this reason, “half-life” is often presented and provides a reference for the amount of time required for the concentration to drop to half of the initial value. Minor manipulation of Equation 16 results in

$$t_{\text{half-life}} = -\frac{\ln 1/2}{\lambda}. \quad \text{Equation 19}$$

Half-life is much easier to visualize than exponential decay rate or mean lifetime. In an analogy, half-life is the time required for a full cup to become half-full. With exponential decay, the time required for a full cup to become half full is the same

amount of time it takes the cup to go from half full to one quarter full, one quarter full to one eighth, and so on. Figure 19 provides a visual summary of a general exponential decay curve and associated terms.

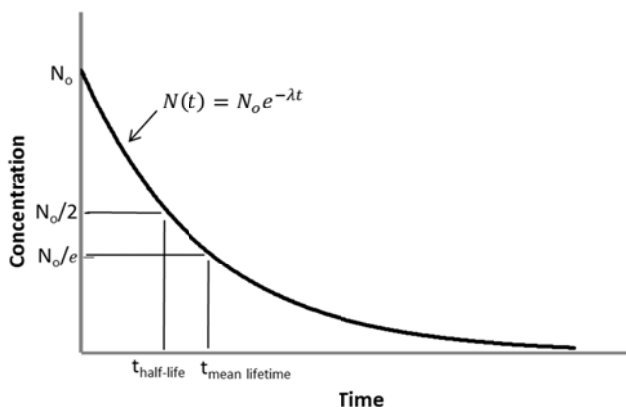


Figure 19. “Ideal” plot of an exponential decay plot with representations of half-life, mean lifetime and respective concentrations.

Exponential decay is often dependent on temperature as first modeled by Arrhenius in 1889. Reactions are accelerated with thermally provided kinetic energy and are modeled by the mean lifetime coefficient associated with the exponential decay. There are a number of reaction models that are variations of the basic Arrhenius equation. These models take into consideration additional factors such as pressure or steric reactions; these models can be drawn on if experimental data shows that some of these additional effects may be relevant. The basic Arrhenius equation provides a general temperature dependent model of exponential decay constant that may be applied to Equation 15 and Equation 16.

The exponential decay constant of Equation 16 changes as a function of temperature, T,

$$\lambda(T) = Ae^{-\frac{E_a}{kT}}. \quad \text{Equation 20}$$

where A is a pre-exponential constant, k is Boltzmann's constant, and E_a is the activation energy of the reaction taking place which is responsible for the concentration as a function of time, $N(t)$. The exponential decay function is often plotted on a semi-log scale as a function of inverse temperature. The function takes a linear appearance on the semi-log scale, Figure 20.

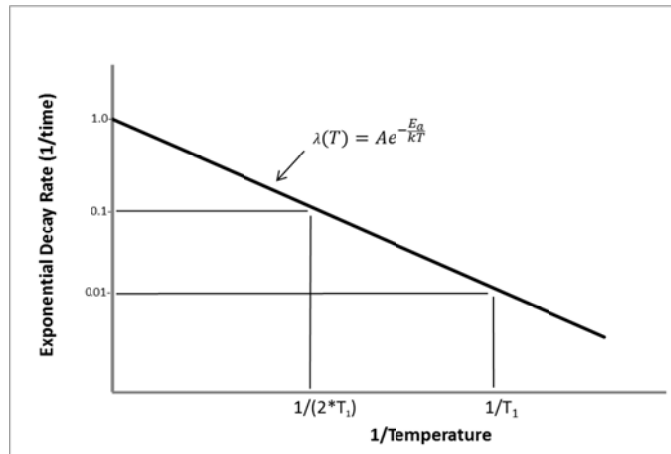


Figure 20. "Ideal" plot of an Arrhenius function on a semi-log plot of exponential decay vs inverse temperature.

2.13 Silicon Etching

Micromachining of the silicon substrate is a critical part of the fabrication process for both microelectromechanical systems (MEMS) and the integrated circuit (IC). In MEMS, the process of machining into the silicon substrate has been used for carving out mechanical devices producing sharp tips, cantilevers, and thin deflecting membranes for atomic force microscopes, pressure sensors, accelerometers, and more. In the IC industry, silicon etching has been used to define MOS geometry, limit diffusions, and provide contact surfaces to specific silicon crystallographic planes[71, 72].

Etching processes can have a wide range of effects, on silicon from producing crystallographic flat surfaces selective to the crystal orientation of the exposed silicon, such as chemical mechanical polishing, to the other end of the spectrum producing porous silicon with hole diameters varying from 2 nm to several microns. The development of porous silicon stems from utilizing the minority carrier diffusion length in the silicon and the oxidation reduction reaction produced at the silicon etchant interface [73].

Etching of silicon can be accomplished with acid solutions such as hydrofluoric/nitric/acetic acid solutions or base solutions such as hydrazine, ethylenediamine pyrocatechol (EDP), tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), and other alkali base solutions. Gas based etching is also a popular method with silicon sublimation via xenon difluoride or plasma based

etching with SF₆ and other associated gases. There is plenty of fantastic in depth literature. There are many great publications providing overviews, in depth theory, and application [74-79].

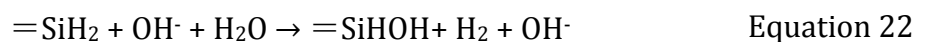
The focus of the following sections will be on anisotropic etching. The process of chemical etching of silicon can be broken down into “chemical” reactions and “electrochemical” reactions. “Chemical” reactions between the silicon and electrolyte will have an exchange of atoms and charge which are exchanged at the interface. The net charge transfer, and thus the net current, between them is zero. The charge transfer between the silicon and electrolyte is measured in “partial currents” where the “anodic current” is the transfer of electrons from the electrolyte to the solid; “cathodic current” is the transfer of electrons from the solid to the electrolyte. Hole transfer is the opposite direction of electron transfer for the respective partial currents. When the charges transfer between the solid and electrolyte is non-zero the reaction is considered to have an “electrochemical” component the reaction. It is this electrochemical component that is frequently used to produce etch stops in silicon micromachining processes. This electrochemical component of the reaction can be produced by many factors; galvanic interaction, external applied potential, photogenerated electrons, or photogenerated electron/hole pairs. Without an externally applied potential the reaction operates at an “open circuit potential” (OCP).

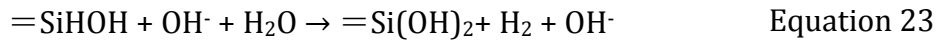
There are multiple steps to the chemical reactions in bulk micromachining monocrystalline silicon using KOH or TMAH/IPA solutions to anisotropically etch

structures into the substrate. The exposed (111) planes in the silicon crystal structure, shown in Figure 21, are less susceptible to chemical reactions with these solutions. KOH solutions typically provide mirror quality machined surfaces. Etching in a (100) plane is favored over etching in a (111) plane by a ratio of 100 to 1 at standard etching temperatures between 70-90°C [80]. KOH etching technology is not CMOS compatible due to the mobile K⁺ ion, and is therefore inappropriate for some applications. TMAH/IPA solutions can provide a 20 to 1 etch selectivity, again favoring etching in (100) planes over (111) planes; and the TMAH/IPA technology is CMOS compatible. The addition of IPA (2-propanol) improves surface quality on the etched planes and is responsible for doubling the etch selectivity available from an equal concentration of TMAH alone [80]. Etching in the direction of the (100) plane is favored over etching in the direction of a (111) plane. Any transient currents between the silicon wafer and the etchant solution are short lived once the wafer is placed in the solution. A simple anisotropic etching set up with the wafer in solution occurs at OCP and is considered a chemical reaction [81]. The complete reaction for the chemical etching of silicon in alkali based solutions is

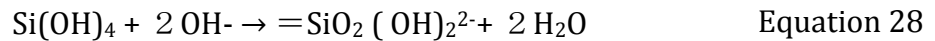
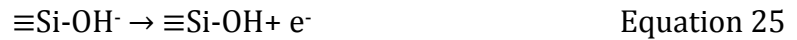
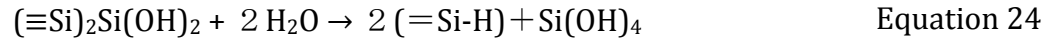


although the chemical process is more complicated and takes place in a number of sequential steps for both the [100] face with two back bonds





and the [111] face with 3 back bonds



as presented by Wind and Hines [82].

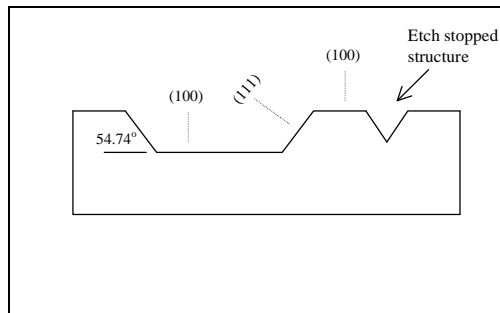


Figure 21. Anisotropic etching characteristics of (100) silicon wafer.

There are a number of factors that play a part in the anisotropic of silicon with alkali based solutions. Silicon atoms along the [100] face have two single back

bonds to silicon atoms within the bulk of the silicon. Each silicon atom along the [100] face surface has two hydrogen terminated surface bonds available for interaction with the etch solution. Silicon atoms along the [111] silicon/etchant interface are more stably bound to the bulk of the silicon substrate with three single back bonds and only one hydrogen terminated bond to react with the etch solution [71]. The activation energy for silicon in KOH is between 0.52 eV and 0.69 eV in the <100> direction and 0.8 eV and 1.0 eV in the <111> direction. There is speculation that there is more at work than a difference in activation energy when it comes to the etch selectivity between the <100> and <111> directions [71]. The range of activation energy is noted to be dependent on the molarity of the KOH solution and the best etching anisotropy occurs in high molarity solutions [83]. A chemical etch stop mechanism has been proposed that [111] silicon's resistance to etching in high concentration KOH solutions is due to water molecules forming a layer with the hydroxylated surface silicon atoms preventing additional hydroxyl ions from reaching the surface to complete a soluble reaction and continue the etching process [83].

The background concentration of dopants, along with crystallographic orientation, in silicon also has an effect on the outcome of chemical and electrochemical reactions [84]. A voltammogram provides valuable insight to different modes of interaction between the silicon and electrolyte exhibiting variations in current density as a function of potential, Figure 22, for KOH solutions and ,Figure 23, for TMAH solutions. Variations of partial currents and their impact

on electrochemical reactions can be understood. The open circuit potential (OCP) is the point where there is no net current between the silicon and KOH. Anodic potentials are positive of the OCP and cathodic potentials are negative of the OCP. The passivation potential (PP) is the point where maximum net current is observed but at which point beyond the passivation potential the silicon surface begins to increase to a point called the Flade potential (FP). At the Flade potential and higher, the etching process is reduced, if not stopped completely as oxidation of the silicon surface dominates [85].

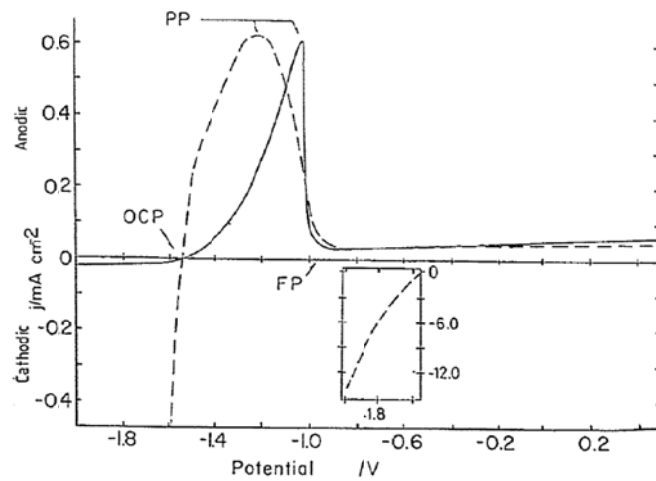


Figure 22. Voltammogram profile for [100], solid line p-type silicon, dashed line n-type silicon in 40% KOH at 60°C [85].

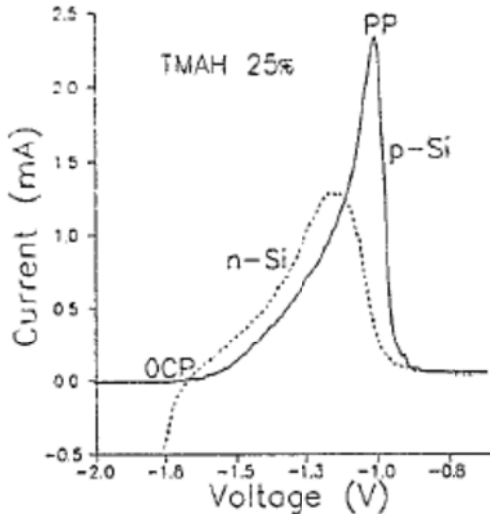
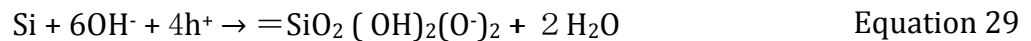


Figure 23. Voltammogram profile for [100], solid line p-type, dashed line n-type silicon in 25% wt. TMAH at 80°C [86].

Although an anodic bias can reduce or even stop etching, anodic etching of silicon can be accomplished when the silicon being etched is anodically biased relative to the OCP. The electrons that are usually at the surface of the silicon at the silicon/etchant interface are drawn into the bulk of the silicon and free holes at the valence band of the silicon interface effectively break the back bonds of the surface silicon atoms.[87]. The reaction for anodic etching is given in



[88], Bressers, et al noted the occurrence of three modes in electrochemical etching. The first mode is chemical only and operates at the OCP. In the second mode the sample is held at a cathodic potential to the OCP and the silicon acts as an electrode in the dissociation of water and produce a large amount of hydrogen. At potentials just anodic to the OCP the current would increase but the etch rate did

not change much from the OCP etch rate. Potentials just anodic to the OCP would increase the oxidation rate of the silicon and assist in producing a hillock free [100] surface. The third mode is a strong anodizing potential. At this potential the current starts to drop off and etching is reduced due to the heavy oxidation of the silicon which produces a barrier to additional etching. The differences between the p-type and n-type potentials are important when looking at p-n junction etch stops. It is also important to keep the potentials measured by voltammogram in consideration when looking at the electrochemical etching differences between [100] and [111] silicon planes [89], Figure 24. Through cyclic voltammetry, etching in KOH of a rectangular region on a [100] silicon wafer shows the effect of current transfer at given potentials between the silicon substrate and a saturated calomel electrode (SCE) constructed of mercury chloride [85, 89, 90]

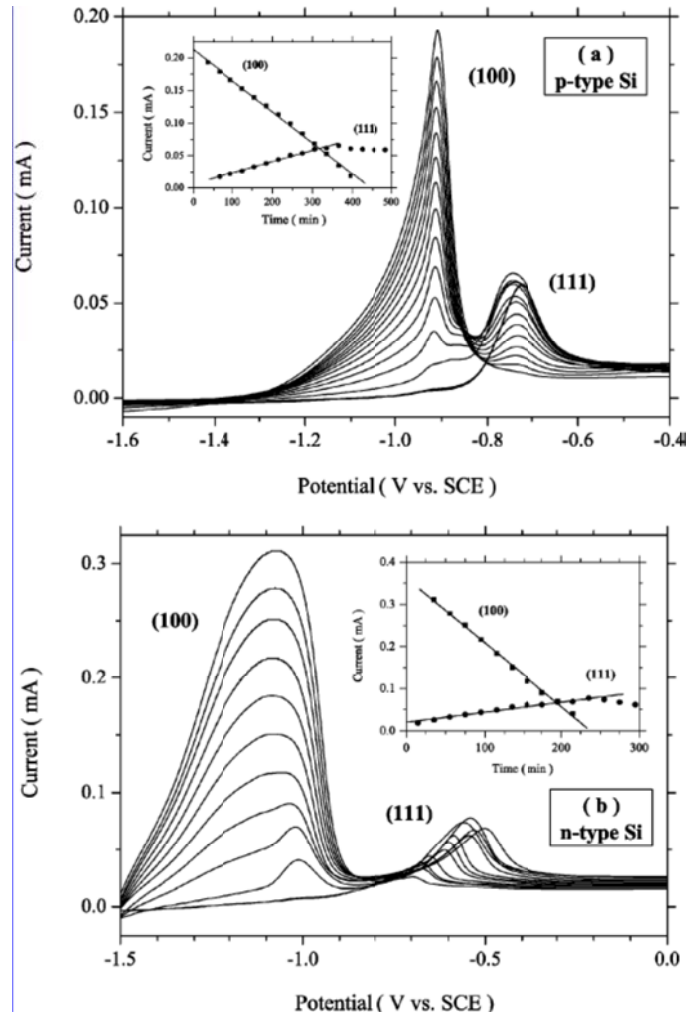


Figure 24. Voltammograms provide insight to etching and passivation potentials of the [100] and [111] silicon faces in KOH for (a) p-type silicon and (b) n-type silicon. Source: [89].

2.14 Band Diagrams of Silicon with KOH and TMAH

Saturated Calomel Electrodes (SCE) made from mercury chloride and the normal hydrogen electrode (NHE) are standards for reference of redox potentials. The standard hydrogen electrode (SHE) is an idealized standard and is useful when

comparing electrochemical redox potentials with vacuum scale of band diagrams. Figure 25 shows the conduction band of silicon to reside at a SHE potential of -0.55 V and the valance band of silicon to reside at 0.50 V [91].

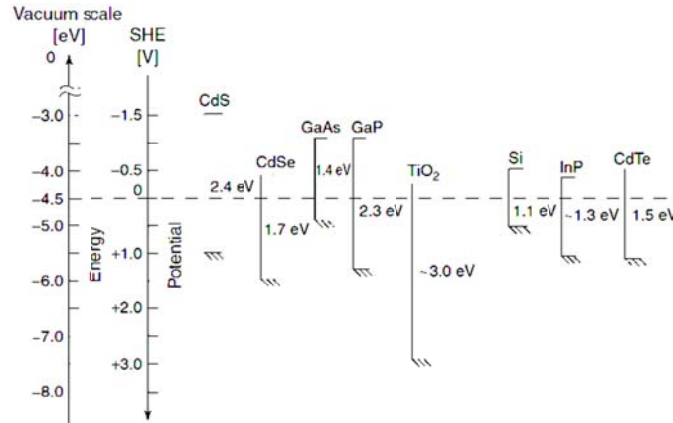


Figure 25. Common semiconductor band gaps are shown relevant to vacuum scale and SHE electrode potential [91].

Figure 26 depicts a band diagram of [100] silicon and a KOH etching solution before making contact. From this band diagram it is apparent that the Fermi energy level of the electrolyte is higher than that of silicon. Submersion of a silicon wafer in the electrolyte creates band bending in a similar manner to a Schottky diode. As shown in Figure 27, band bending due to a transfer of charge at the interface occurs for both p-type and n-type silicon. The surface states of silicon at the liquid interface also produces trap locations deep in the silicon band due to dangling and back bonds [71].

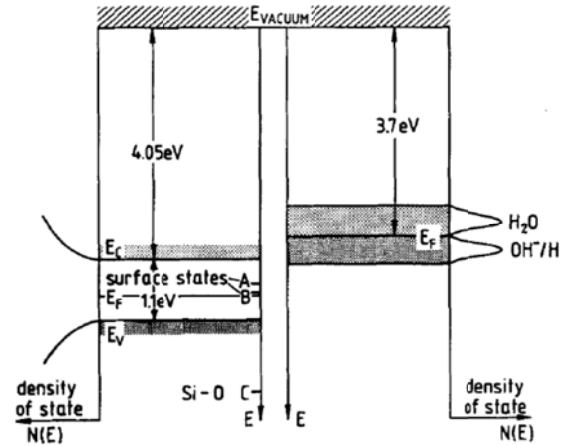


Figure 26. The band diagram and density of state diagram for silicon and KOH alkali based etch solution respectively. Source: [71]

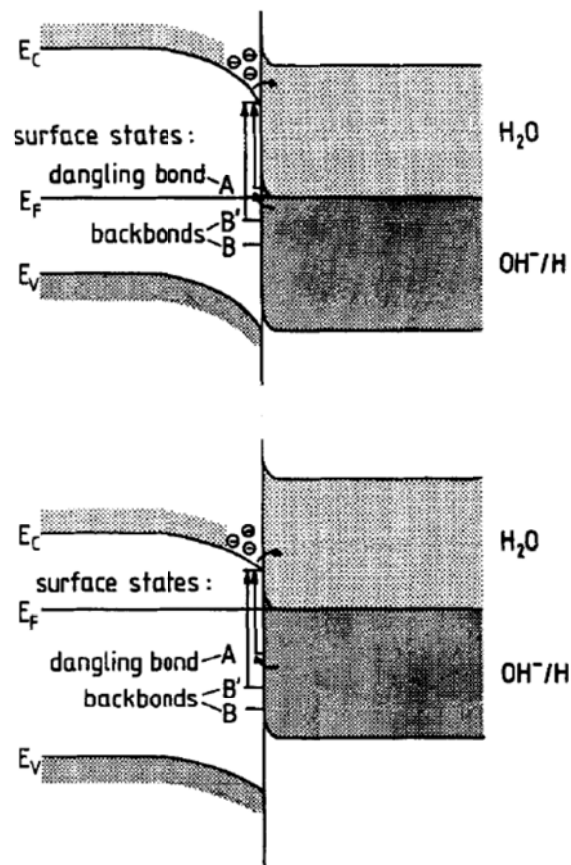


Figure 27 Band diagram once the silicon is in contact with KOH alkali based etchant; (top) p-type silicon, (bottom) n-type silicon. Source: [71]

TMAH is another common etchant used with silicon and a band diagram is constructed in the same fashion as for KOH, Figure 28. The Fermi level of TMAH is below the Fermi level for n-type silicon and moderately doped p-type silicon at the open circuit potential (OCP). According to Nemirovsky, the band diagram of silicon with the electrolyte etchant correctly shows the Fermi levels of the silicon and electrolyte are not aligned and therefore that the system is not in thermal equilibrium [92]. The OCP is generated by the two stage chemical reaction; first, the reduction of water to hydroxyl ions and hydrogen gas; the second, the oxidation of silicon. These two reactions make up the silicon etching process in alkali based solutions.

Reactions can occur between a semiconductor and electrolyte utilizing both valence and conduction bands between the electrolyte or a single band. In this case, the valence band is responsible for the transfer regardless of whether it is n-type or p-type [93],

Figure 29. As the oxidizing agent is reduced in the electrolyte of this example, additional holes drift in to the semiconductor and a quasi-Fermi level is generated in the n-type semiconductor.

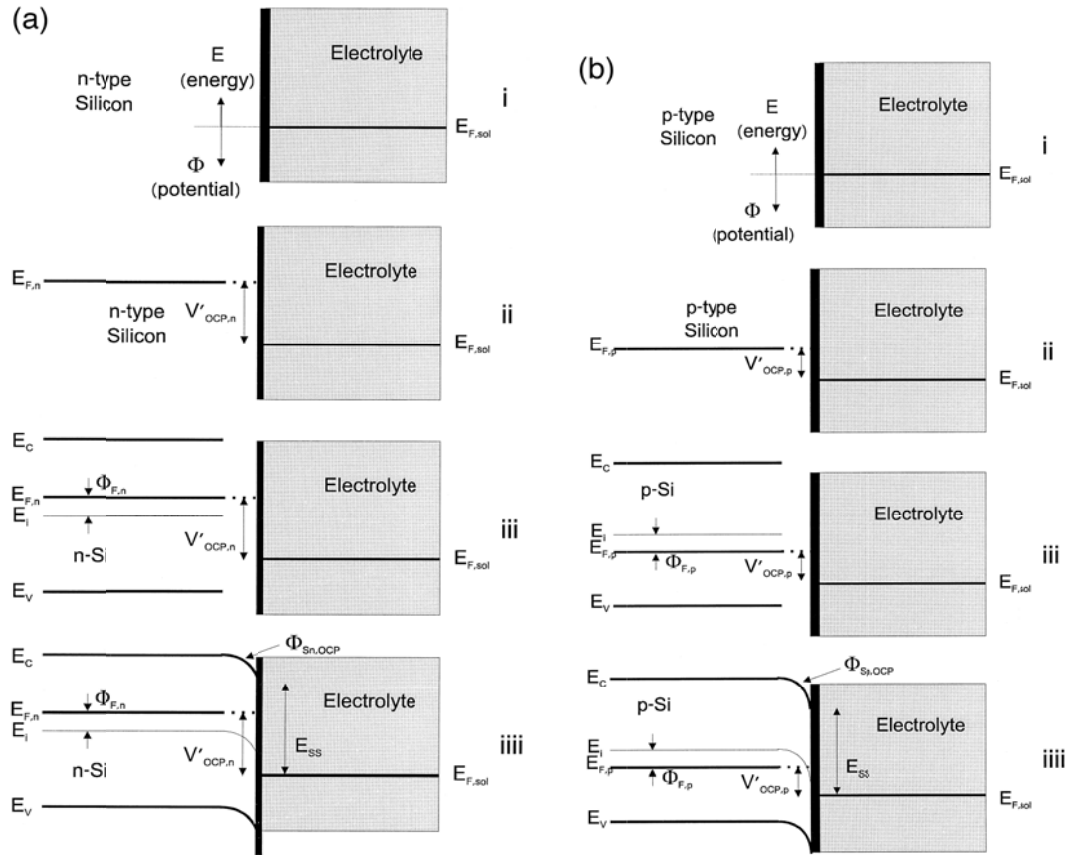


Figure 28. Band diagram of silicon with 25% TMAH etch solution. (a) n-type silicon/alkali electrolyte (b) p-type silicon/alkali electrolyte. Source: [92].

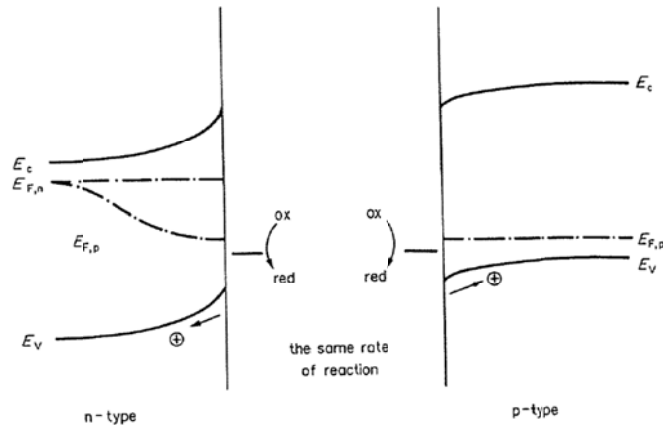


Figure 29. Semiconductor Fermi levels shown at the interface of electret redox reaction [93].

Looking at the chemistry of anisotropic etching in will provide the background required to understand how an MIS structure can promote an etch stop. The first thing to look at for a P-type wafer is its natural unbiased potential in an anisotropic etchant such as KOH, Figure 32. Free electron carriers accumulate at the region of silicon up to the silicon/etchant interface as is needed to keep the Fermi level constant between materials. This happens with N-type silicon as well but to a lesser extent [19]. The hydroxyl ions in the wafer play the critical role in etching crystal silicon in the (100) face. A silicon atom from the solid face bonds with two hydroxyl groups and become soluble to the solution leaving two electrons. These electrons return to the base solution producing additional hydroxyl ions to continue the reaction with silicon. The supply of electrons to the base etchant is crucial to providing a continuous etch process. In the use of an electrochemical etch stop, this supply of electrons from the silicon to the etchant is truncated by adjusting the potential of the silicon substrate to an anodic bias relative to the etch solution, Figure 31.

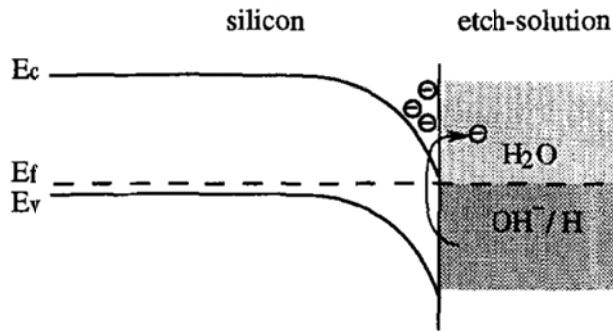


Figure 30. P-type silicon in anisotropic KOH etchant. Source: [19].

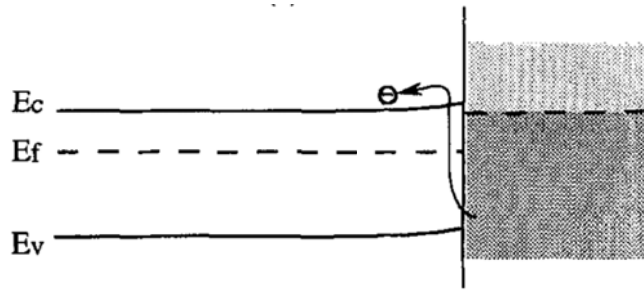


Figure 31. Anodic bias to P-type silicon in anisotropic KOH etchant. Source: [19]

2.15 Bias Effects on Anisotropic Etching of Silicon

As one of the few alternatives to a timed etch stop, the anodic bias of the substrate is a valuable tool, aiding in the high dimensional tolerance machining of many silicon based MEMS devices. In many cases, external power sources and electrodes are needed to implement this anodic bias; a potentiostat is used in conjunction with a platinum reference electrode and a silver/silver chloride counter electrode. Often great effort is put in to ohmic contact doping and complicated jigs. These high quality electrical contacts are needed to make an effective and consistent contact to the wafer [94]. The jigs are required to separate electrical contacts from the etch solution. The process of electrochemical etch stop becomes expensive and cumbersome.

An etch stop is only valuable if it can be implemented at the correct time or in the correct location. An anodic potential in the form of a reverse bias P-N junction can be tuned to precise locations and biased to produce well controlled silicon membranes using etch stop techniques. A drawing of the fundamental set up for an

electrochemical etch stop is shown in Figure 32. The silicon etching stops within the p-type silicon just before the metallurgical junction depth and models silicon etchant solution as a bipolar junction transistor (BJT). The etch solution is the emitter, the remaining p type silicon near the end of etch is the base, and the n-type silicon is the collector. The base-emitter is forward bias and the base collector is reverse bias, Figure 33. This puts the system in a forward active mode and requires a constant supply of current to maintain the etch stop [95-97].

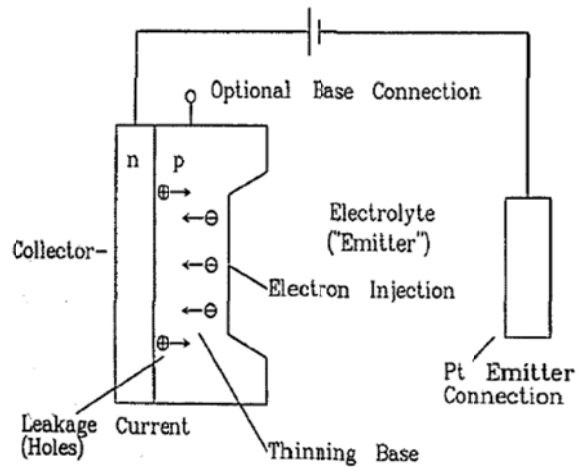


Figure 32. npn BJT model of pn junction of electrochemical etch stop [96]

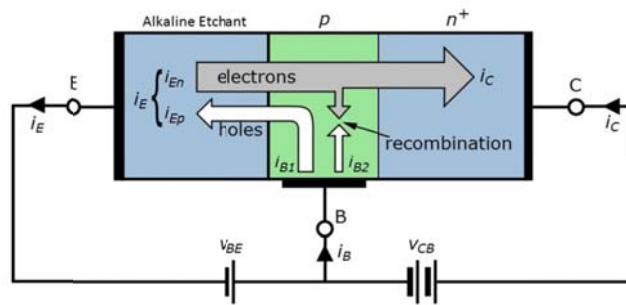


Figure 33. NPN BJT schematic shown with the base-emitter forward biased and the base-collector reverse biased [86].

Acero was able to show that TMAH can be used in an electrochemical etch stop similar to KOH. The study included TMAH solutions of 25% and 2.5% wt, with and without IPA. An n-type membrane was fabricated using this etch stop using a PN junction as the depletion region. The etch stop setup shown in Figure 34 makes use of a three electrode configuration where the n-type region of the silicon is connected to the potentiostat. The reverse bias between the p-type and n-type regions is controlled by maintaining a sufficient positive potential, from n-type to p-type material, on the silicon (work electrode) relative to the TMAH etch solution, (reference electrode). It was noted by the authors that the electrochemical etch stop of n-type silicon occurs at potentials anodic to the OCP in this configuration and that the current through the work electrode peaks at the onset of silicon passivation. Ashruf point out the advantage of TMAH over KOH in an anodic etch stop process in that TMAH is very sensitive to silicon oxides as a masking layer, where the selectivity between [100] silicon and silicon oxide is much lower with KOH etchants [81]. A four electrode configuration has also been developed, Figure 35. The four electrode configuration provides better etch stop control and allows the reverse bias of the pn junction to be maintained independently of the silicon-etchant potential [98].

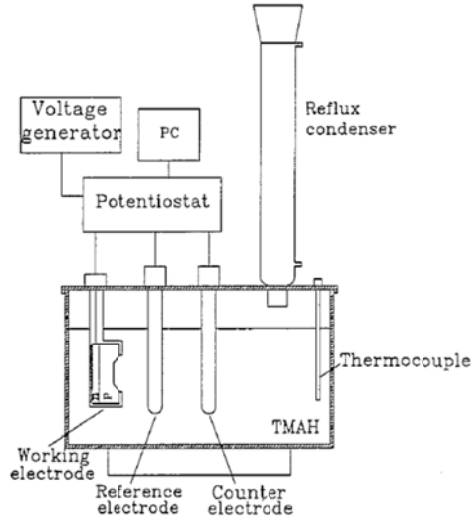


Figure 34. TMAH based three-electrode electrochemical etch stop using a pn junction [86].

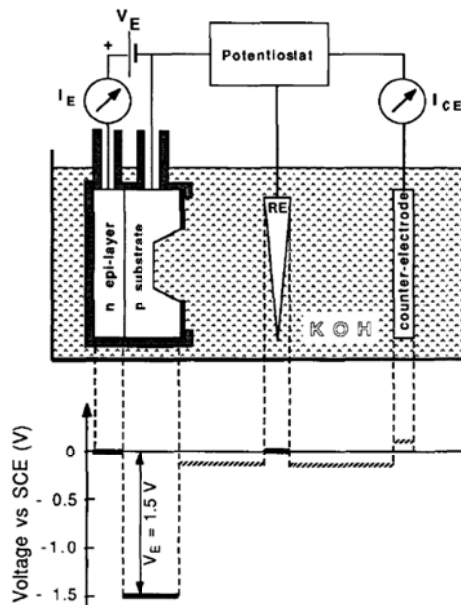


Figure 35. Biased PN junction etch stop in KOH using a four electrode configuration. The relative potentials of the work electrode (pn junction), reference electrode, and counter electrode are shown from left to right. Source: [98]

The metal insulator silicon (MIS) etch stop configuration in p-type silicon is a variation of the reversed bias p-n junction etch stop. The strong inversion layer of the biased MIS produces the depletion region.. In the case of the MIS etch stop (shown in Figure 36), it is critical that the voltage (V_2) is tuned and maintained between the silicon wafer and the etchant solution for the anodic oxidation of the substrate to occur just prior to reaching the depletion region. It is in this region where the quasi-Fermi level of free electrons decreases and electrons are no longer injected back into the solution to propagate the production of hydroxides needed for silicon to continue etching [99]. The current flow between the silicon substrate and the etchant is maintained by the external voltage, V_2 , applied between the silicon substrate and etchant, draws the anodic current required to stop the etch once the etch front reaches the strong inversion region of the MIS maintained by external bias V_1 .

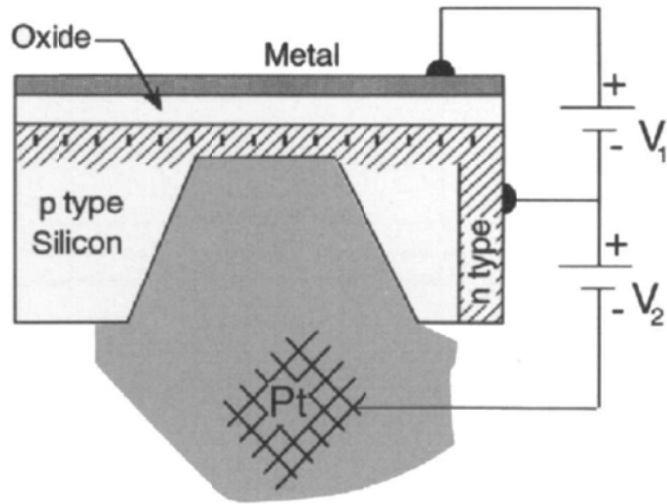


Figure 36. A MIS electrochemical etch stop configuration is shown for p-type silicon. A region of n-type silicon is produced for electrical contact to the silicon substrate. A platinum electrode is submerged in the etchant to bias the silicon-etchant interface [99].

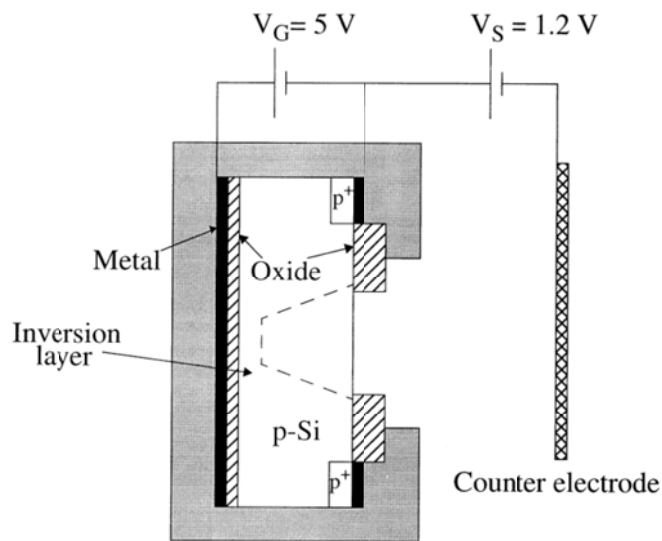


Figure 37. MIS etch stop produced by inversion layer [87].

3 FABRICATION AND METHODS

The methods for fabricating and characterizing the electret and the implementation of the electret as an electrochemical etch stop are presented. First, the deposition of the PECVD silicon nitride and silicon oxide deposition and substrate are defined. Second, the method of direct contact thermally assisted poling is covered followed by the evaluation of the film's effective surface voltage. Subsequently, the process for optimizing electret activation for negative potentials and the accelerated lifetime testing methods for both positive and negative potentials are described. Lastly, the details for testing the electret as part of an electrochemical etch stop with TMAH is outlined.

3.1 PECVD Deposition of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$

P-type, boron doped, (100) silicon wafers ($d = 100 \text{ mm}$, $t = 525 \text{ }\mu\text{m}$) and a resistivity of 1-10 ohm-cm was used in all of the experiments to characterize the electret activation process and isothermal potential decay.. A cladding of silicon nitride and silicon oxide films, similar in construction to that used in SONOS devices, was produced. Specifically, the dielectric was created by coating a film of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$, at a nominal thickness of 1650 nm/250 nm/28 nm respectively, on

the silicon substrate via PECVD. The silicon nitride and silicon oxide films were deposited at the same temperature, but at different pressures, 550 mtorr and 1000 mtorr, respectively, using the silane/argon, ammonia, nitrous oxide and nitrogen gas rates shown in Table 1. The silicon nitride was deposited using RF/LF power pulse parameters of 20W for 30 sec/50W for 2 seconds to minimize film stress in the silicon nitride while the silicon oxide was processed with 20W of RF power only. Prior to the thermally assisted poling, the SiO₂/Si₃N₄/SiO₂ films were placed on a 200°C hotplate in atmosphere for one hour to remove excess water which had been absorbed by the SiO₂/Si₃N₄/SiO₂ from the air. This “bake out” was followed up with a hexamethyldisilazane (HMDS) spin coat at 4000 RPM for 10 seconds to produce a hydrophobic surface on the SiO₂/Si₃N₄/SiO₂ and prevent future water absorption from humid air.

Table 1. PECVD process parameters

	Temp. (°C)	Pressure (mtorr)	RF		LF		5% SiH ₄ /Ar (sccm)	NH ₃ (sccm)	N ₂ O (sccm)	N ₂ (sccm)
			Power (W)	Pulse (sec)	Power (W)	Pulse (sec)				
silicon oxide	350	1000	20	-	-	-	170	-	710	-
silicon nitride	350	550	20	30	50	2	200	50	-	200

The film thickness of each SiO₂ and Si₃N₄ layer was determined by first running preliminary wafers with a single film layer of SiO₂ or Si₃N₄ and measuring selectively etch and unetched regions by surface profilometry (Dektak 8, Veeco Inc.,

Plainview, New York). The film thickness of each SiO₂ and Si₃N₄ layer was determined by first running preliminary wafers with a single film layer of SiO₂ or Si₃N₄. PECVD silicon oxide deposition was performed for 25 seconds, 25 minutes, and 30 minutes using one silicon wafer for each respective time. PECVD silicon nitride deposition was performed for 5 minutes and 30 minutes using one wafer for each respective time. The wafers were subsequently photolithographically patterned and the PECVD film was selectively etched in BOE until it became hydrophobic. The photoresist was stripped from the substrate in acetone and rinsed in DI water. The step height of the PECVD film was then measured in five locations by contact profilometry (Dektak 8, Veeco Inc., Plainview, New York). The five locations consisted of the center and four quadrant locations approximately 2cm from the wafer edge. A full cassette of 25 substrate wafers were run as a batch once the required deposition times had been determined.

3.2 Wafer Level Thermally Assisted Poling of Electret

The thermally assisted poling was performed in an anodic bonder (SB-6e, SUSS MicroTec AG, Garching, Germany) by placing a 2" 100 P-type silicon wafer in contact with the 100 mm silicon substrate containing the multilayer PECVD deposited silicon nitride and silicon oxide films, creating a "wafer stack" with the PECVD film between the two polished faces of the silicon substrates, Figure 38. A schematic is shown in Figure 39. Under a 5 mtorr vacuum with nitrogen purge, each wafer stack in the study was subjected to a range of voltages (60 V – 540 V) to identify the

optimum maximum voltage needed for activation. The voltage was applied to the top wafer acting as a cathode for applying the bias across the PECVD film during electret activation. During the activation process, the wafer stack was heated to a maximum temperature over a range (150°C - 210°C) to produce an electret with a negative effective surface voltage. With the full voltage applied, the wafer dwelled at the elevated temperature for one, three, or 5 hours and then allowed to cool to 40°C before the applied voltage was removed.

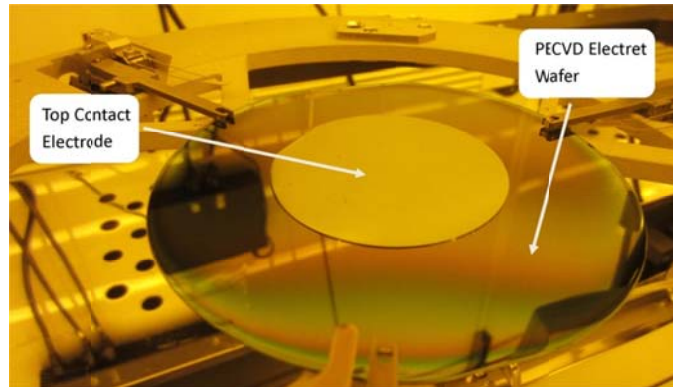


Figure 38. 100 mm diameter silicon wafer with PECVD dielectric film is loaded with 2" "cathode" wafer in SUSS SB-6e bonder tooling.

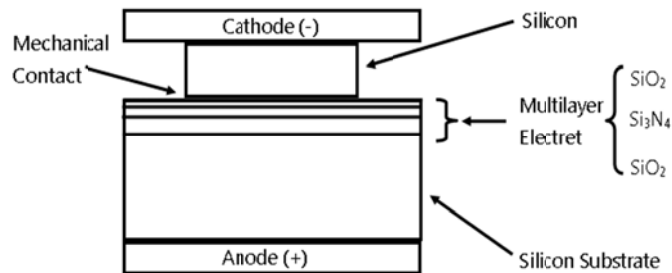


Figure 39. Schematic of the setup for the thermally assisted poling of the multilayer film stack on a silicon wafer.

As an example, a typical thermally assisted poling process flow consisted of generating a negative surface voltage in the electret when the wafer stack was subjected to an applied voltage of -180 V while being heated to 170°C, Figure 40. Under the applied voltage, the wafer dwelled at 170°C for one hour and was then cooled to 40°C before removal from the clamping electrodes of the SUSS bonder. Once the sample was activated, it was removed from the SUSS bonder and the top electrode silicon wafer was pried with wafer tweezers from the PECVD film and substrate. The substrate was once again spin coated with HMDS at 4000 RPM to treat the surface to assure that it will remain hydrophobic. Every sample in this study was activated in a similar manner; however, the time, temperature, and applied voltage were varied to determine the optimum electret activation treatment.

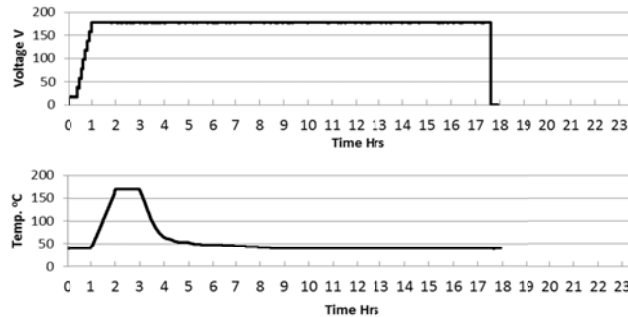


Figure 40. Example temperature and voltage magnitude profile used for the electret activation process in the SUSS bonder.

3.3 Electret Measurement and Evaluation

An electrostatic voltmeter (Model #279, Monroe Electronics, Inc., Lyndonville, New York) was used to measure the effective surface voltage (ESV) of the electret film after activation. The probe was maintained at a distance of two millimeters from the electret surface and measured a 2 mm diameter field at any given location. The $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ substrate was mapped with the use of a microscope stage. The theory of operation for the electrostatic voltmeter was presented in section 2.5 - "Electric Displacement Field". A detailed map of the electret's effective surface voltage across the wafer was used to evaluate the average maximum ESV and to generate a detailed contour plot, Figure 41. The average of the five highest ESV data points defined the overall maximum ESV achieved under the particular process parameters. Each data point represents a reading at a pitch of 1.5x1.0 cm of the 100 mm diameter wafer.

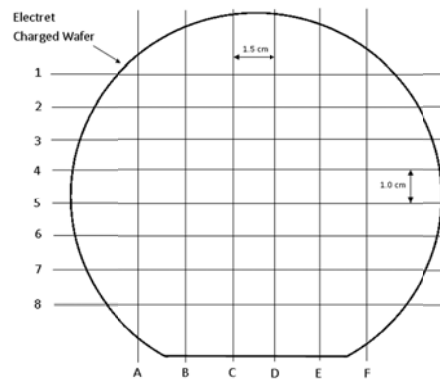


Figure 41. ESV measurements were made over the wafer surface at the intersections of the alpha numeric grid at a pitch of 1.5 cm and 1.0 cm.

3.4 Process Optimization, Design of Experiments

A 2^3 full factorial design of experiments (DOE) was implemented to evaluate the main effects of the thermally assisted poling process; temperature, process time, and applied voltage [100]. The boundary conditions on the DOE were 170°C and 190°C; one hour and five hours; and, -180 V and -300 V. A midpoint value of 180°C, -240 V and a three hour dwell time, respectively, was also tested. The midpoint value provides additional data which can be used to confirm the variable effect, variable interactions, and the possibility of nonlinear effects. Each sample was mapped and the average of the five highest similar ESV data points were used in the DOE. The term “similar” signifies that the effective surface potential measured on the surface of the film possessed the same polarity as the potential applied by the cathode. For this DOE model, “similar” referred to a negative potential. An additional analysis was performed to evaluate the five highest complementary ESV data points used in the DOE; where the term “complementary” signified the effective surface potential opposite of the cathode potential, i.e. a positive potential for this DOE model.

Based on the results of the 2^3 full factorial DOE, Section 3.4 - “Process Optimization, Design of Experiments”, both temperature and applied voltage significantly contribute to the production of the electret ESV. A single factor DOE was performed for the temperature and voltage variables to determine the extent that the resulting ESV is affected by temperature and voltage. The effect of the process temperature

was characterized at 150°C, 170°C, 190°C and 210°C. Similarly, based on the 2³ DOE, all of the experiments in this sequence were performed with a potential of -180 V applied to the electret surface for a one hour dwell period. In addition to the temperature dependent single factor DOE, the effect of applied voltage was characterized in an extended single factor DOE for processing voltages of -60 V, -180 V, -300 V, -420 V and -540 V. All of the experiments in this voltage dependent sequence were conducted at 170°C with a five hour dwell period.

3.5 Electret Characterization

Temperature has been shown to have one of the greatest effects, other than humidity, on decreasing the useful lifetime of an electret [7]. Thus, experiments were designed to determine the isothermal potential decay (ITPD) of the ESV produced under different processing conditions. An extrapolation of the temperature dependence for the ITPD data was performed to obtain the useful mean lifetime of the ESV provided by the electret for typical operation temperatures. A description of sample preparation and experiments performed has been defined below.

3.5.1 Isothermal Potential Decay Sample Preparation

The DOE using ITPD data required the decay rate to be evaluated at a number of elevated temperatures. To this end, eight wafers were prepared at the wafer level in accordance with the process standards presented in section 0 - "

PECVD Deposition of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ “ and section 3.2 - “Wafer Level Thermally Assisted Poling of Electret” . Four of the eight wafers were activated at the applied potential of positive 300 V and the four remaining wafers were activated at negative 300 V to determine the effects of polarity on the performance of the electret. Five samples were cleaved from each of these wafers to perform the ITPD experiments for each wafer at five different accelerated aging temperatures (325°C, 300°C, 275°C, 250°C, and 200°C) with the goal of extrapolating the room temperature lifetime coefficients and activation energy from the Arrhenius plots. In order to perform an analysis of variance (ANOVA), a minimum of four wafers were needed to demonstrate statistical significance for the temperatures tested.

3.5.2 Isothermal Potential Decay Experiments

To perform the ITPD, a sample electret from each respective wafer was placed on the hot plate (Dataplate PMC 720, Barnstead/Thermolyne, Dubuque, Iowa), at one of the specified accelerated aging temperatures listed above, and the respective ESV was immediately measured by the electrostatic voltmeter with a distance of 2 mm between the probe and the center of the sample. Effective surface voltage measurements were continually acquired as the sample “aged” at the elevated temperature to produce decay plots. After all samples were tested, a nonlinear regression was performed for each sample treated to determine the “best fit” for the data to an exponential decay equation in the form of

$$ESV(t) = ESV_0 e^{-t/\tau} \quad \text{Equation 30}$$

This relationship yielded the lifetime coefficient, τ , a characteristic of each sample that was determined from the ESV as a function of time. Since the starting ESV value varied between electret samples, the ESV was normalized to an initial value of one, the exponential term was unaffected by this normalization. Plots of the exponential decay are presented in Figure 67 and Figure 68 in section 4.2 - "Characterization and Optimization of Electret Formation Process".

3.5.3 Evaluation of Isothermal Potential Decay Trials

The exponential decay data for all samples was utilized to generate a best-fit Arrhenius equation

$$\lambda = \frac{1}{\tau} = A e^{-E_a/kT} \quad \text{Equation 31}$$

where A represents the number of decay interactions possible over a given time; the exponential function represents the probability of a decay interaction taking place as a function of temperature, T , and the activation energy, E_a , of the system and Boltzmann's constant, $k=8.617\text{E-}05$ eV/K. This equation was used to extrapolate the decay rates of the ESV for temperatures that lied outside the range of accelerated aging tests.

3.6 Application of Electret as an Electrochemical Etch Stop

This project investigated the use of the electret as a source of electric bias in an electrochemical etch stop. As stated in the Background (or Literature Review) chapter, based on previous work by others[86, 87, 95, 96, 98, 101], electrical potentials have been demonstrated to provide the electric field required for the strong inversion of a semiconductor that is required for an electrochemical etch stop. However, these methods have implemented traditional electronic equipment external to the substrate or galvanic effects to provide the necessary bias to produce the required strong inversion within the semiconductor. The trapped charges of the electret provide the permanent bias needed in a MOS bias etch stop, making this the first process of its type to operate without an external power supply. An electrical bias generated electrostatically produces an electrochemical etch stop without requiring additional doping of the silicon and also provides future possibilities for a patterned etch stop. For completeness, experiments were run with the electret in both polarities. In each configuration, the electret was deposited directly on the back-side of the silicon wafer being etched, Figure 42. The electret was activated to produce a negative or positive ESV. It was expected that this etch stop will work if the electric field from the electret is significant enough to bias the silicon into a depletion mode at the silicon-electret interface. The methods for this etch stop study is presented in three parts. Preliminary methods cover the preparation of the wafer and die is presented. Second, the actual etch study on

batch treated positive, neutral and negative electrets. Lastly, real time effective surface voltage measurements are made as the etch progresses.

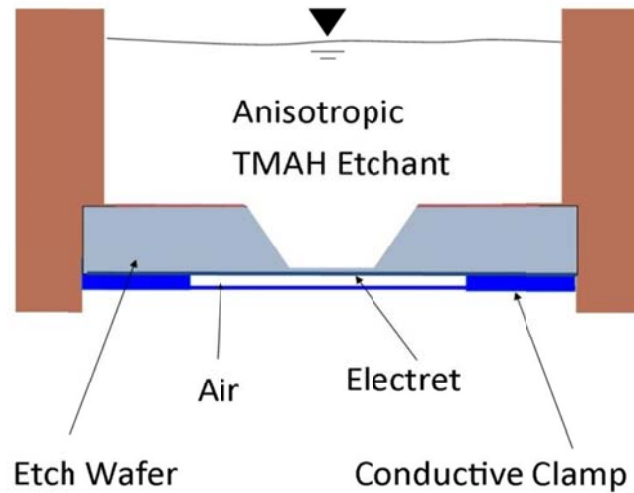


Figure 42. Anisotropic wet etch with electret on etch wafer.

3.6.1 Wafer and Die Preparation for Electrochemical Etch Stop

The electret is susceptible to neutralization and charge masking. Because of this, the sequence of activating the electret in a device process sequence is critical. It is not possible to activate the electret film prior to dicing due to exposure to water and debris during the dicing process. Because of the electret's susceptibility to charge neutralization, dicing was completed prior to electret activation for all experiments conducted to determine the effectiveness of the electret as an electrochemical etch stop.

All wafers used for the etching study consisted of silicon substrates, double-sided polished, P-type, boron doped, (100), with resistivity ranging from 15 ohm*cm to 25 ohm*cm, and nominal thickness 380 μm . The substrates are coated with the PECVD oxide/nitride/oxide layer 1650 nm/250 nm/28 nm thick respectively, in accordance to the deposition parameters presented in section 0 – “

PECVD Deposition of $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ ”. Each PECVD coated wafer was diced with a dicing saw (DAD 321, Disco Inc., Japan) to 20 mm by 20 mm die. Each wafer yielded 9 electret samples for etch stop testing. In order to acquire sufficient data to perform an analysis of statistical significance, a total of 9 square openings (800 μm to a side) were patterned in the PECVD multilayer film on the secondary polished side of each die on the wafer using conventional contact lithography techniques, providing 9 etch windows for producing cavities from subsequent anisotropic etching, Figure 43.

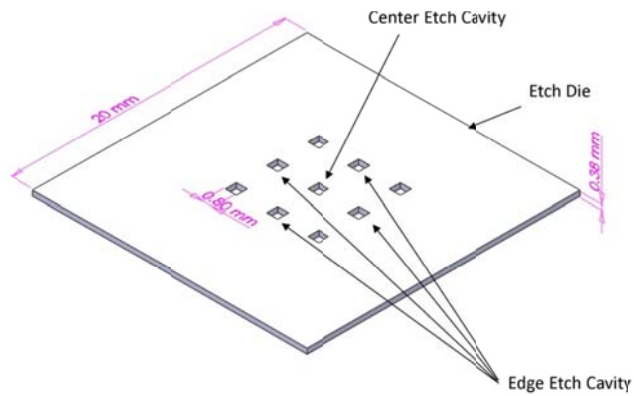


Figure 43. Each of the etch die contain 9 etch cavities for evaluation of effects of the electret on the progression of silicon etching in the cavities.

A die level variation of the electret activation was performed under atmospheric conditions for one hour at 170°C with an applied voltage of magnitude 300 V on a hot plate (PMC 720). The top contact electrode was diced to 13 mm by 13 mm from a p-type (100) silicon wafer with a 1-20 ohm*cm resistivity. Both the PECVD coated die and the top contact die were placed on a hot plate at 200°C in atmosphere for 1 hour for a dehydration bake and followed up with a HMDS drop and nitrogen gun dry. To activate the electret, the PECVD coated die was placed on an aluminum faced hot plate (Dataplate PMC 720) set to 40°C and the polished face of the electrode die was centered on top. A small piece of indium was placed on the electrode die to improve contact between the die and the activation probe and small bare silicon pieces are pressed to the edge of the electret etch die to improve grounding contact, Figure 44. A power source meter (#2410, Keithley Instruments, Inc., Cleveland, OH) was used to apply a +/-300 V potential between the aluminum face of the hot plate and the electrode die. The hot plate temperature was elevated to 170°C at a ramp rate of 100°C/hr and allowed to dwell for 1 hr. Subsequently, the hot plate was allowed to cool and the 300 V potential was removed when the temperature fell below 100°C. The electrode die was pried from the electret substrate in order to measure the electret's ESV with the electrostatic voltmeter.

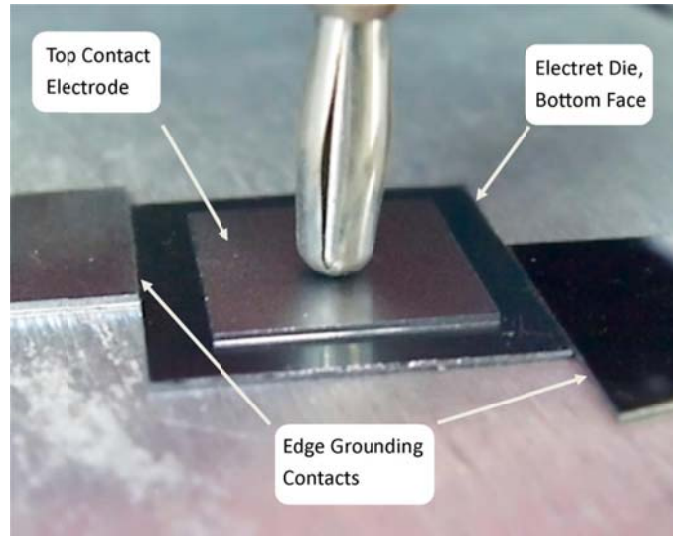


Figure 44. Die level electret activation was performed with sub-sized silicon die on the PECVD film. Small piece of silicon are placed to the edge of the die to improve ground contact between the hot plate and electret die.

A total of three wafers were processed for these etch stop experiments. From each wafer, 3 die were fabricated with a targeted positive ESV of +150 V; 3 die were fabricated with a targeted negative electret ESV of -150 V; and the three remaining die from each wafer were uncharged (0 V) and used as control samples during the etch rate experiments.

3.6.2 Calculations for the Justification of Strong Inversion

Based on prior works of p-n junction and MOS style etch stops discussed in the background, it is critical that this ESV meets or exceeds the potential required to ensure a state of strong inversion within the p-type silicon at the dielectric silicon interface for positively charge electret samples. An evaluation of the band diagram

for electret-semiconductor interface provided confirmation that the die for this anisotropic etch study were considered viable samples with an ESV in excess of 150 V, -150 V, or within +/- 10 V for the 0 V control samples. An electret oxide semiconductor (EOS) band diagram looks much like a MOS band diagram, Figure 42. The energy bands, conduction and valance, for a given semiconductor and dielectric will behave identically to bias generated by the net charges on a metal of a MOS structure or fixed "trapped" charges at the surface of the dielectric in an EOS structure. The maximum depletion width, W_m , can be used as a first approximation for the minimum etch stop, as it has been previously reported that anisotropic etching stops at or before reaching the depletion region for p-n junctions and MOS style etch stops [19, 87]. For example, 143 nm is calculated as the maximum depletion width for a p-type [100] silicon wafer with a background impurity, N_A , of $1.5(10)^{16}$ atoms/cm³ based on a resistivity, ρ , of 10 ohm-cm is 0.30 μ m with the potential between E_i and E_F , given as ϕ_F , is 0.3578 V.

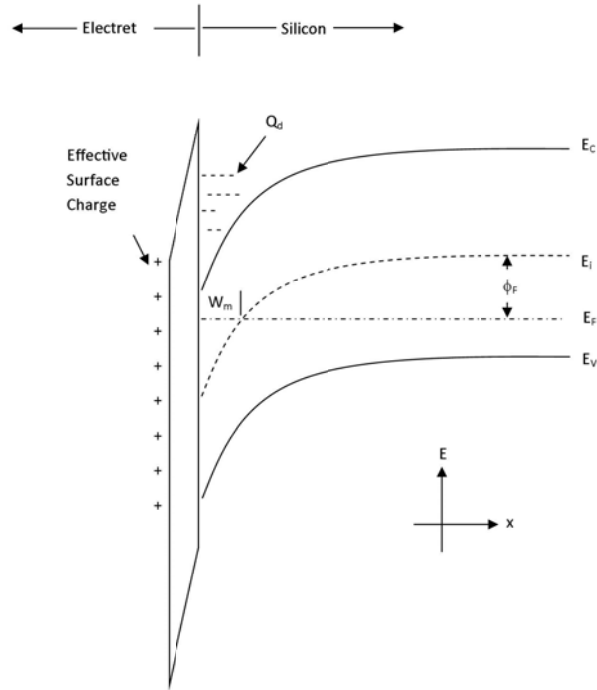


Figure 45. Electret Oxide Semiconductor band diagram in a state of strong inversion.

The maximum depletion width, W_m , is

$$W_m = 2 \sqrt{\frac{\epsilon_s \phi_F}{q N_a}} \quad \text{Equation 32}$$

where ϵ_s is the permittivity of silicon, q the charge of an electron, and the potential is ϕ_F ,

$$\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i} . \quad \text{Equation 33}$$

The minimum surface charge, Q_d , required to drive the depletion width to the maximum value is 34 nC/cm^2 given by

$$Q_d = -qN_aW_m . \quad \text{Equation 34}$$

The minimum ESV needed to provide the surface charge required for the maximum depletion width was

$$ESV = -\frac{Q_d}{C_i} + 2\phi_F . \quad \text{Equation 35}$$

It was necessary to determine the minimum acceptable ESV to implement the condition of strong inversion and maximum depletion width; the conservative estimate was to consider the thickness of the capacitor dielectric, d , to be the complete PECVD film stack thickness, which in the case of this study, was 1928 nm . A conservatively low permittivity of $3.45(10)^{-11} \text{ F/m}$ was used as the permittivity of the film stack, ϵ_i , based on the literature of permittivity for PECVD films. The insulator capacitance, C_i , was calculated using the relationship:

$$C_i = \frac{\epsilon_i}{d} \quad \text{Equation 36}$$

In this case, given the values mentioned above, the capacitance was calculated to be 1.79 nF/cm^2 , which corresponds to a required minimum ESV for a state of maximum depletion width to be $+19.8 \text{ V}$. Therefore, it was anticipated that a strong inversion state was achieved since the targeted 150 V ESV was over seven times the minimum

value necessary to create the charge required for producing the maximum depletion width.

3.6.3 Electrochemical Etch Stop Etch Cells and Environmental Control

In order to carefully control the etch stop process, a custom etch cell chamber was designed and fabricated to meet the following criteria:

- Maintain chemical and structural integrity at elevated temperatures of 120°C;
- Conduct heat from the hot plate evenly to the etch solution;
- Limited chemical interaction between etch cell and solution;
- Capable of holding 20 ml of etching solution;
- Prevent evaporation of the solution during the etch; and,
- Hold a 20 mm by 20 mm silicon die with thickness ranging from 350 nm to 550 nm.

To meet the requirements, the etch cells were machined from virgin PTFE with a matching PTFE cap. The O-rings provide the liquid seal between the etch cell and silicon die. The base of the etch cell was machined from 50 mm OD and 12 mm ID, 316 stainless steel. An isometric drawing of the etch cell design is shown in Figure 46.

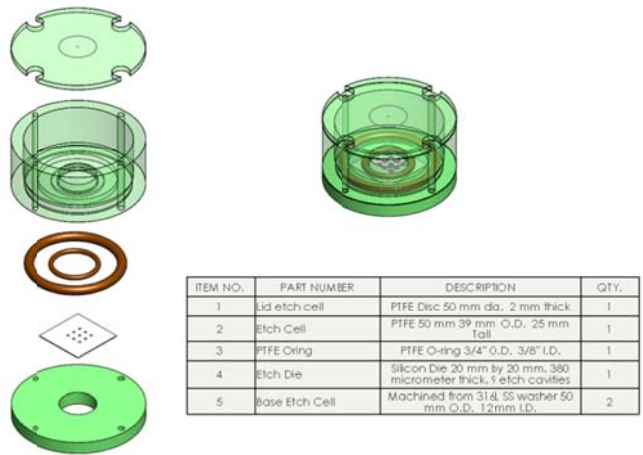


Figure 46. Isometric drawing of the etch cell assembly with sample die.

Temperature uniformity is critical to a successful evaluation of the effect of the electret on etch rates. To this end, the etch cells are placed in an enclosure during etching to promote a uniform temperature surrounding the etch cell by thermal conduction and minimize convective influence that occurs in a fume hood. The assembly of the etch cell, etch cell lid, graphite sheets, and aluminum enclosure on the hot plate are shown in Figure 47. The enclosure itself is a cast aluminum electrical enclosure (CN-5711, BUD Industries, Willoughby, OH) with final box dimensions of 5½" wide by 8½" long and 1½" tall. A flexible 1/8" thick graphite sheet was used as an interface between the ultraflat hot plate and the aluminum enclosure due to its excellent heat conduction properties and its ability to deform to shape to insure uniform contact between surfaces. Similarly, an additional sheet of graphite was placed between the base of the box and the etch cells.



Figure 47. Nine etch cells are shown on the hot plate in the aluminum enclosure with the lid off to the side. One etch cell is shown with the PTFE lid removed, showing the silicon die and its 9 respective etch cavities.

3.6.4 Electrochemical Etch Stop Timed Study Overview

Cavities were etched in the silicon die at regular time intervals of 60 min from the front side of the wafer in 25% tetramethylammonium hydroxide (TMAH) at 60°C. The back-side of the wafer consisted of a PECVD deposited oxide-nitride multilayer film in positive, negative, and neutral charged conditions. As the etched silicon membrane approached the back-side electret film, the etch depth was measured with an optical profilometer (Newview 7300, Zygo Corporation, Middlefield, CT) at each time interval. The etch rate of samples with positive, negative, and neutrally charged electret activation were evaluated at each etch

interval to determine if there is any statistical difference in etch rate as the silicon etch plane approaches the back side charged electret film.

The etching process consisted of loading the die in their respective etch cells, which were then placed in the etching enclosure. The etching enclosure was set on top of the hot plate that was operating at 70°C. Based on other etch stop methods that took advantage of MOS inversions or p-n junction biases, there was no anticipated effect of the electret on the etch rate when the distance between the (100) etch face and the electret film was greater than 20 μm . Subsequently, the silicon die were each etched in 20 ml of 25% TMAH etch to a cavity depth of 300 μm for a single etch period of 18 hours, leaving 60 μm to 80 μm of silicon remaining to investigate the effect of the electret charge on the silicon etch rate process. After the 18 hr etching step, the depth of five etch cavities in each die was recorded with the Zygo optical profilometer. The depth of the center etch cavity and the four edge cavities in the 3 by 3 array were measured, Figure 43. Each cavity was measured from each of its four edges, Figure 48. Thus, a total of 20 etch depth measurements were acquired for each die.

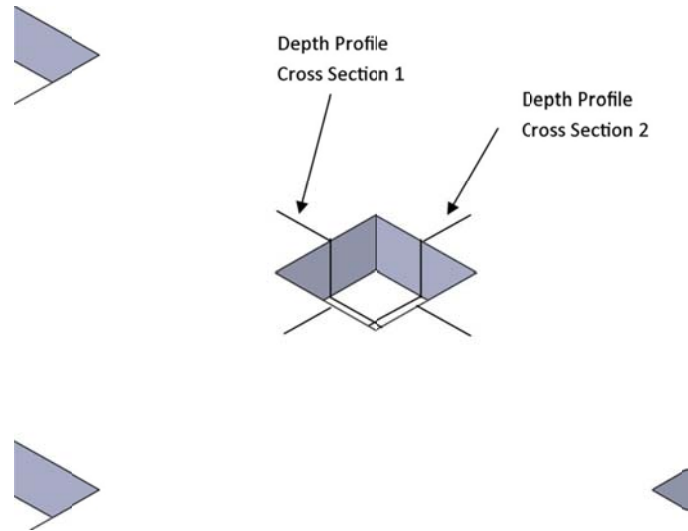


Figure 48. The surface topology is measured for five of the etch cavities on each die. Two cross sections of each cavity measured provide a total of four etch depth measurements.

After the initial 18 hr etch depth measurements were completed, the samples located in the etch cells were loaded with fresh 25% TMAH and the remaining silicon was etched using the same protocol described above for the initial etch, except this time the samples were etched for 60 minute instead of 18 hrs. At the end of the 60 minutes, the TMAH was discarded from each cell, and the cell was rinsed with DI water and dried with compressed air. The step heights of the five cavities in each sample were again measured with the optical profiler. The etch depth before and after the 60 minute etch process was used to determine an effective etch rate of the samples for every hour of etching. This etching process cycle was repeated 15 times until the etched sample reached the PECVD multilayer electret or the sample failed by leakage. The etch depth data was evaluated as a function of time to

determine if there was a statistically significant variation in etch rate as the TMAH silicon interface approaches the depletion region or enhanced carrier region of the silicon caused by the electret charge.

3.6.5 Confirmation of Environmental Etch Conditions

A uniform distribution of heat was confirmed via thermal imaging of the aluminum lid and PTFE lids removed. To capture these images, the samples were allowed to reach steady state, which took about 15 minutes, as the assembly was heated to 70°C on the hot plate. A partial immersion thermometer was used to confirm that the temperature of the solution was uniform amongst the test cells. While the temperature set point for the hot plate was 70°C, all of the sample solutions measured 60°C +/- 1°C.

3.6.6 Electret Stability During Anisotropic Etching

Due to the susceptibility of the electret charge to be neutralized when exposed to liquids, it was important to monitor the ESV during the anisotropic etching process. Therefore, the last set of etching experiments, done with the third wafer in the study, were performed in order to measure the ESV from the electret side before and after the silicon etch step. Utilizing the opening in the stainless steel base of the etch cell, the ESV measurements were collected on each die in the third trial before the silicon etch proceeded. This ESV measurement was considered a modified ESV due to the interference in the electric field caused by the surrounding metal of the

grounded washer through which the measurement was being taken, Figure 49. The measurement procedure of the modified ESV was followed again at the end of the etching procedure to confirm that the electret charge was still in place after the etching process. Due to resolution limitations of the electrostatic voltmeter, it was still not possible to determine the durability of the electret charge in regions where the complete backing of the substrate had been etched through. This information is tabulated in the results to provide evidence that the electret charge was maintained throughout the etching process.

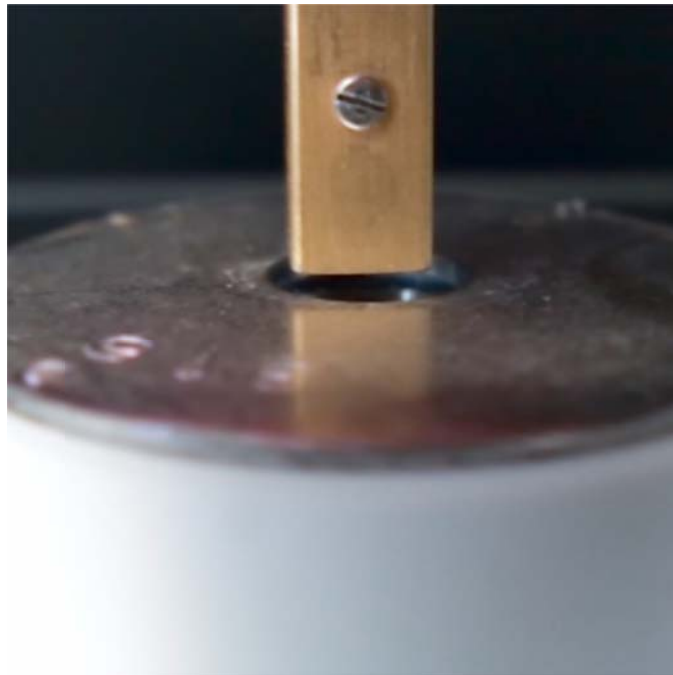


Figure 49. A "Modified" ESV measurement is made after each etching period to confirm that the electret is still active.

4 RESULTS

$\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}_3\text{N}_4$ multilayer electrets were successfully fabricated by PECVD deposition and subsequent thermally assisted poling using the techniques described in Chapter III. The thermally assisted poling process was optimized, with a 2^3 full factorial DOE and two single factor DOEs, to achieve the maximum ESV for negatively charged electrets. The ESV of the electret was characterized by isothermal potential decay (ITPD) to determine the activation energy of the trapped charges in the electret and extrapolate the mean lifetime of the ESV at room temperature and operating temperatures. In addition, the implementation of the electrets as an anisotropic electrochemical etch stop are presented and described below.

4.1 Wafer and Film Dimensions

The PECVD $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ multilayer was deposited to a nominal thickness of 1650 nm/250 nm/28 nm respectively as measured by contact profilometry of single layer films on silicon substrates. The substrates were P-type, boron doped, (100) silicon wafers ($d = 100$ mm, $t = 525$ μm) with a moderate doping resulting in a resistivity of 1-10 ohm-cm. The resulting silicon oxide deposition for 25 seconds, 25

minutes, and 30 minutes is shown in Table 2. The resulting silicon nitride deposition for 5 minutes and 30 minutes is shown in Table 3.

Table 2. Silicon oxide thickness measurements, mean and standard deviation.

Silicon Oxide Thickness (nm)							
Deposition Time	Measurement Location on Wafer					Average (nm)	Std dev (nm)
	#1	#2	#3	#4	#5		
25 sec	28	29	26	27	29	27.8	1.2
25 min	1605	1711	1713	1721	1578	1665.6	61.2
30 min	2069	2045	1926	1897	2066	2000.6	73.8

Table 3. Silicon nitride thickness measurements, mean and standard deviation.

Silicon Nitride Thickness (nm)							
Deposition Time	Measurement Location					Average (nm)	Std dev (nm)
	#1	#2	#3	#4	#5		
5 min	45	43	43	44	41	43.2	1.3
30 min	263	245	254	248	252	252.4	6.2

4.2 Characterization and Optimization of Electret Formation Process

The significance of temperature, process time, and applied voltage on the ESV produced by the thermally assisted poling process was investigated using a 2^3 full factorial DOE. Each of the nine $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ PECVD coated wafers was subjected to thermally assisted poling in the SUSS bonder with the smaller 2" wafer on top acting as the contact cathode. In this DOE, trials were run with all combinations of process times of one and five hours; process temperatures of 170°C and 190°C; and applied activation potentials of 150 V and 300 V. An additional trial was performed with a midpoint value of three hrs. 180°C, and 240 V for the process time, temperature and applied activation potential, respectively. The average of the 5

peak values for each wafer was used to provide a meaningful value that is representative of an area significant to provide a yield of useful devices in a fabrication process. The results for the ANOVA of the 2^3 full factorial DOE are presented in Table 4. The five peak negative ESV values measured in the ESV contour mapping of the each surface were averaged as the data points of the “cube” plot, Figure 50; “interaction effects” plot, Figure 52; and “main effects” plot, Figure 51. Evaluation of the P-values for the ANOVA on the 2^3 full factorial DOE for negative ESVs provide the following:

- 1) curvature (or nonlinear) effects were not significant;
- 2) the time-temperature interactions were very significant;
- 3) the temperature-applied voltage interaction was marginally significant;
- 4) applied voltage main effect were very significant;
- 5) time main effect was marginally significant.

A maximum effective surface voltage of -236.2 V was achieved at the maximum activation temperature of 190°C with the maximum applied process voltage of 300 V and the maximum process time of five hours in the DOE. From this result, it was concluded that increasing the ESV by extending these process parameters could provide insight to the processing limits for electret activation.

Table 4. Factorial Regression: Peak versus time, temperature, voltage, CenterPt
Analysis of Variance

Source	DF	Adj SS	Adj MS	F-Value	P-Value
Model	8	46839.6	5855.0	6.20	0.000
Linear	3	24533.1	8177.7	8.66	0.000
time	1	7344.1	7344.1	7.78	0.008
temperature	1	624.1	624.1	0.66	0.422
voltage	1	16564.9	16564.9	17.54	0.000
2-Way Interactions	3	20261.1	6753.7	7.15	0.001
time*temp	1	17056.9	17056.9	18.06	0.000
time*voltage	1	348.1	348.1	0.37	0.548
temp*voltage	1	2856.1	2856.1	3.02	0.091
3-Way Interactions	1	828.1	828.1	0.88	0.355
time*temp*voltage	1	828.1	828.1	0.88	0.355
Curvature	1	1217.3	1217.3	1.29	0.264
Error	36	33999.6	944.4		

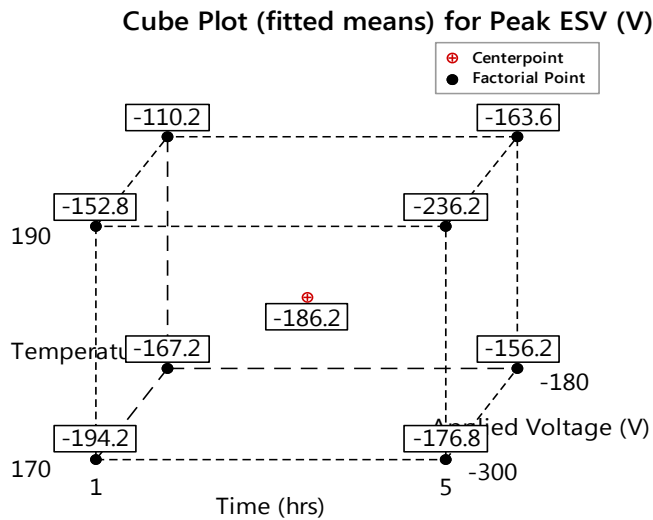


Figure 50. Negative potential ESV “cube” plot of the 2^3 full factorial DOE given the effects of temperature ($^{\circ}\text{C}$), time (hrs), and applied voltage (V) on the ESV (V). The averages of the five peak ESV values for each wafer are shown at the corners and center of the plot.

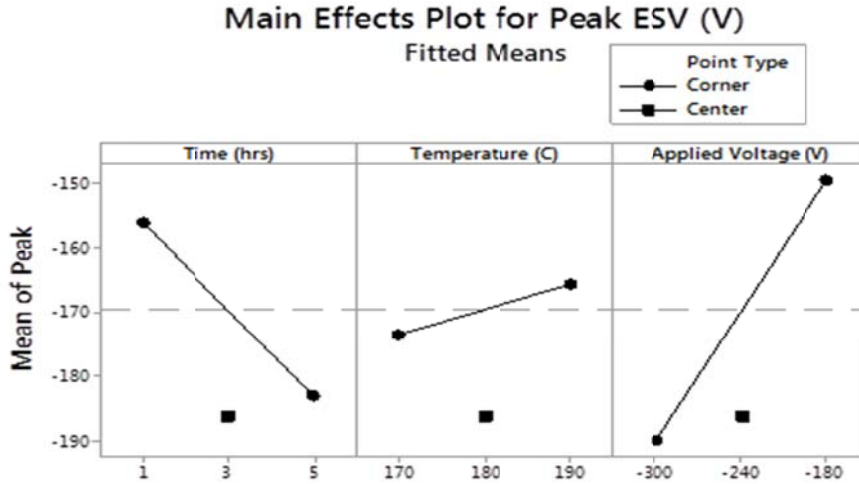


Figure 51. The “main effects” plot of the negative ESV as a function of temperature (°C), time (hours), applied voltage (V).

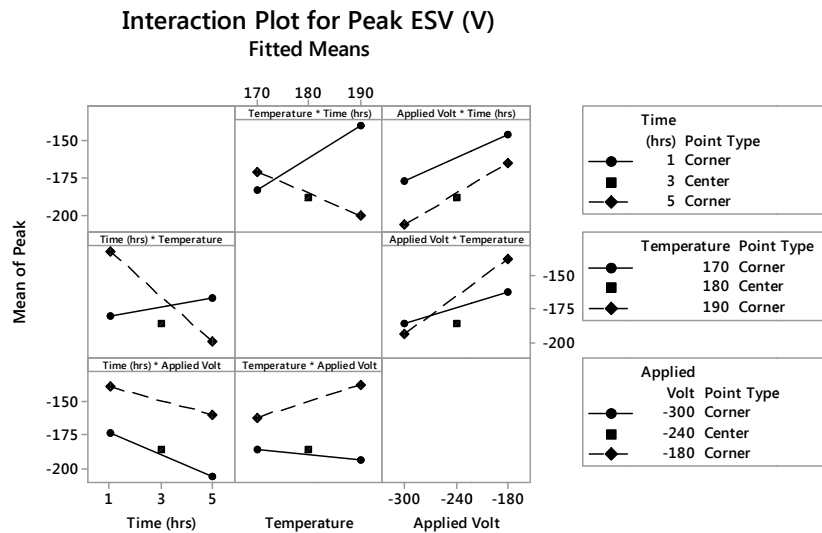


Figure 52. Negative potential ESV “interaction” plot of temperature (°C), time (hours), applied voltage (V).

Once the 2³ full factor DOE had been completed, it was important to extend the range of the applied temperature and applied voltage process parameters to

determine the optimal process parameters for the ESV of the electret. A single factor DOE was performed for the applied temperature and applied voltage parameters by running additional experiments extending the testing range of the applied temperature from 70°C to 230°C and the applied voltage from 60 V to 540 V. Full wafers were processed in the SUSS bonder using the standard PECVD SiO₂/Si₃N₄/SiO₂ (1650 nm/250 nm/28 nm) on a 100 mm p-type silicon substrate used in the initial 2³ full factorial DOE. The top five negative ESV measurements from the full contour plots are averaged resulting in a single data point for each wafer in the extended single factor DOEs. The single factor DOE for applied temperature showed that the applied temperature linearly increased over the range of 70°C to 210°C (Figure 53). However around 190°C, the ESV did not display a linear relationship and tended to deteriorate as the process temperature increased further to 230°C. This could be attributed to applied voltages approaching the breakdown voltage of the dielectric PECVD film with applied voltages at elevated temperatures. This would be an expected limit since the high electric fields in the PECVD film have been shown to be responsible for the generation of charge trapping sites in the electret [102]. The additional traps generated at elevated temperatures decreases the resistivity of the PECVD film, resulting in a current load beyond the capacity of the SUSS bonder power supply at the applied voltage. The extended single factor plot of ESV due to applied voltage is shown in Figure 54. The single factor DOE for the applied process voltage illustrated a clear trend, where an increase in the applied process voltage resulted in an increase in ESV. While it has

been documented that electric field stressing of the dielectric is responsible for trap generation [66], these traps may not be filled by mobile charges unless the electret is processed at higher temperatures. Additionally, there is a risk that a high electric field induces a breakdown in the PECVD film. Once a low resistivity path is produced in the thin film it is not possible to maintain the high potential during activation and this limits both the yield and ESV produced. This occurred at the highest applied voltage of -540 V. The first trial at this applied potential had an abrupt drop during the activation process and the maximum current supplied by the SUSS bonder was insufficient to maintain the -540 V. The resulting ESV of this first trial was -112.2 V. A second trial was run successfully producing an average peak ESV of -226.8 V, providing the highest mean ESV for all samples produced throughout these studies. Based on the assumptions and calculations presented in section 2.6-“Effective Surface Voltage Electret Measurement” and Equation 13, an effective planar charge density of 4.7 mC/m^2 was produced for this ESV of -226.8 V assuming that the charge resides at the silicon nitride-silicon oxide (blocking layer). A trial had been conducted at an applied potential of -600 V, data not shown, but the sample suffered a complete electrical breakdown. The SUSS bonder supplied the maximum 10 mA current but the resulting applied potential was 0 V. The maximum effective surface voltage -226.8 V was produced with a blocking oxide produced by PECVD and 1650 nm thick. The maximum ESV was limited by this electrical breakdown of the blocking oxide. The maximum producible ESV can be increased

by increasing the thickness of the PECVD blocking oxide or by producing a blocking oxide with a higher breakdown voltage.

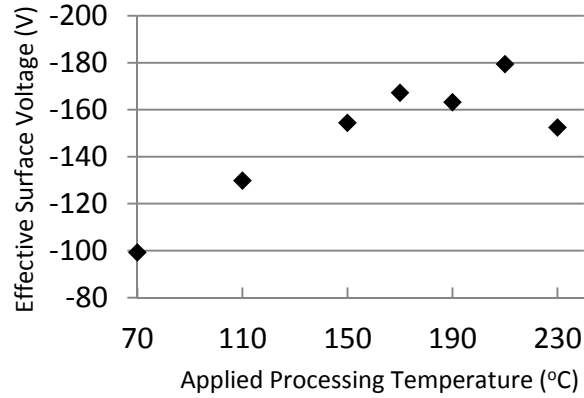


Figure 53: Effective surface voltage as a function of applied process temperature for samples activated at 170°C for five hours. samples activated at 180 V for one hour.

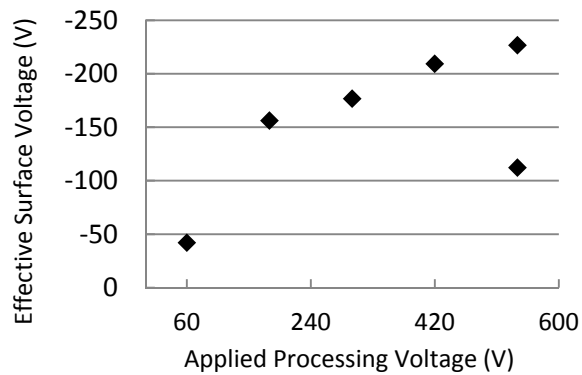


Figure 54: Electret surface voltage as a function of applied process voltage for samples activated at 170°C for five hours.

As previously described in Chapter III, contour maps of the activated electret wafers were created for each variation in process parameters (Figure 55 -Figure

61). The average of the five maximum ESV values for the sample run at each DOE process parameter is represented at the corners and center of the 2^3 full factorial DOE cube. In examining the contour maps, it can be seen that the effective surface voltage matches the polarity of the contact wafer when the contact wafer was used as the cathode. The regions of the contact wafer and electret film on the substrate acted as a poor conductor, resulting in the ESV having the same polarity as the applied potential. In addition, regions of a positive ESV, opposite the polarity of the cathode polarity were also seen; however, these occurred in areas that were not in direct contact with the cathodic contact wafer. The regions of positive ESV were due to the gap between the upper cathode electrode and the silicon substrate acting as a capacitor.

As a result, two polarities, positive ESV and negative ESV, were created on the electret surface in a single process of applying a negative applied voltage during activation. This dual-polarization was accomplished in regions of contact versus noncontact applied voltages provides a great opportunity for enabling the programming of electrostatic fields on the surface of the electret. For example, this process may be used to pattern (or stamp) a specific electric field on a device for a particular application, such as energy harvesters [15] and acoustic sensors [44]. Additional studies are required to determine the limitations of this programming capability to take into account the effects of feature size, field magnitude, and charge bleeding on the surface of the electret, but these were not investigated at this time.

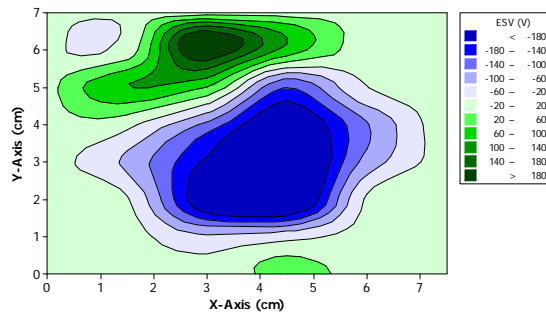


Figure 55. ESV contour plot with electret activation at -300 V, 5 hrs, 190°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

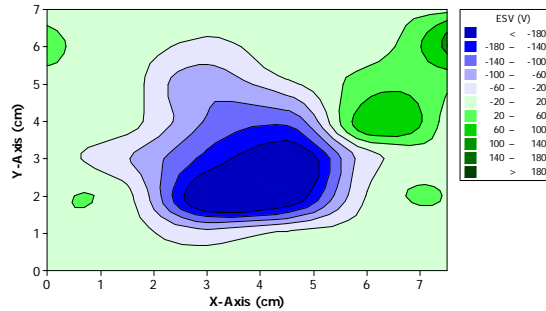


Figure 56. ESV contour plot with electret activation at -300 V, 1 hrs, 170°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

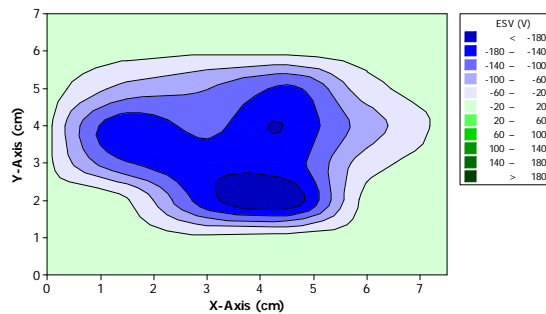


Figure 57. ESV contour plot with electret activation at -300 V, 5 hrs, 170°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

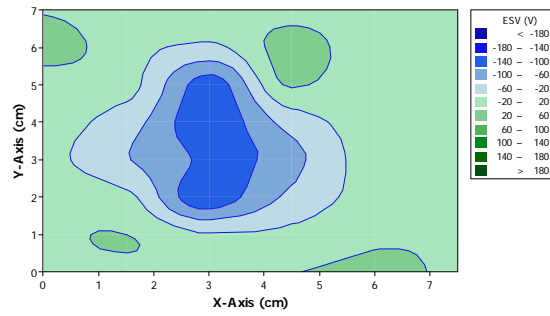


Figure 58. ESV contour plot with electret activation at -180 V, 1 hrs, 190°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

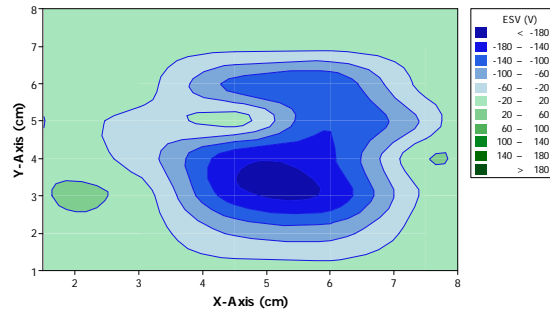


Figure 59. ESV contour plot with electret activation at -180 V, 5 hrs, 170°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

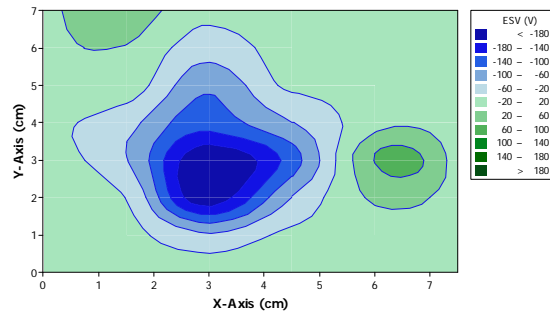


Figure 60. ESV contour plot with electret activation at -300 V, 1 hr, 190°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

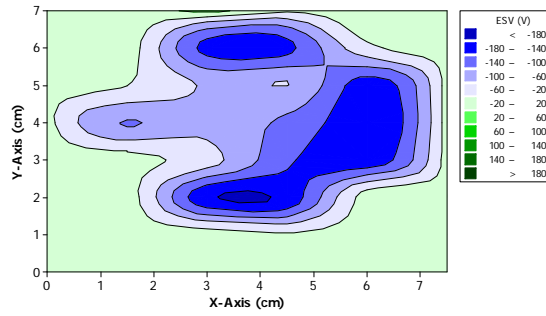


Figure 61. ESV contour plot with electret activation at -180 V, 1 hr, 170°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

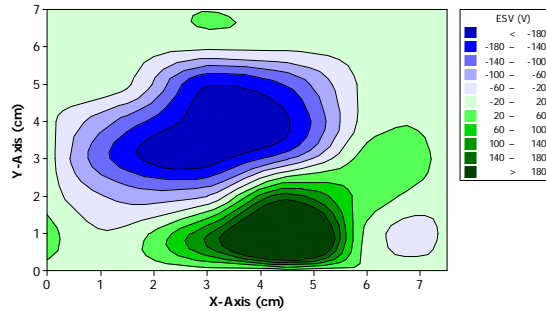


Figure 62. ESV contour plot with electret activation at -225 V, 3 hrs, 180°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

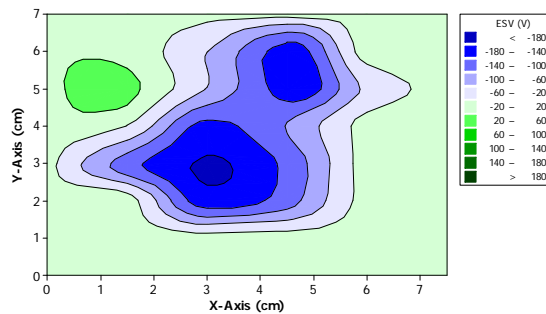


Figure 63. ESV contour plot with electret activation at -180 V, 5 hrs, 190°C. The color coded legend on the right provides the scale of the ESV at 20 V increments.

The 2^3 full factorial DOE was originally designed to investigate the dependencies of process temperature, time, and negative applied voltage on the negative ESV produced during electret activation. Review of the ESV contour maps showed that not only were there negative ESVs produced as expected, but there were also regions of positive ESV produced in regions of the wafer that were not in direct contact with the cathode used to bias the PECVD film. The data from these experiments was repurposed to investigate how these process parameters affect the performance of producing a positive ESV with a negative applied voltage. The results for the ANOVA of the 2^3 full factorial DOE are presented in Table 5. The five peak positive ESV values measured in the ESV contour mapping of the each surface were averaged as the data points of the “cube” plot, Figure 64; “interaction effects” plot, Figure 65; and “main effects” plot, Figure 66. Evaluation of the P-values for the ANOVA on the 2^3 full factorial DOE for positive ESVs provide the following:

- 1) applied voltage provided a marginally significant effect;
- 2) the time, temperature, and applied voltage produced a 3-way interaction that was significant.

Table 5. Factorial Regression: Peak positive ESV versus time, temperature, voltage

Analysis of Variance

Source	DF	Adj SS	Adj MS	F-Value	P-Value
Mod	8	100875	12609.4	3.94	0.002
Linear	3	14933	4977.7	1.56	0.217
time	1	17	16.9	0.01	0.942
temperature	1	5244	5244.1	1.64	0.208
voltage	1	9672	9672.1	3.03	0.091
2-Way Interactions	3	8004	2667.9	0.83	0.484
time*temp	1	6052	6051.6	1.89	0.177
time*voltage	1	314	313.6	0.10	0.756
temp*voltage	1	1638	1638.4	0.51	0.479
3-Way Interactions	1	14364	14364.1	4.49	0.041
time*temp*voltage	1	14364	14364.1	4.49	0.041
Curvature	1	63574	63574.0	19.89	0.000
Error	36	115086	3196.8		
Tota	44	215961			

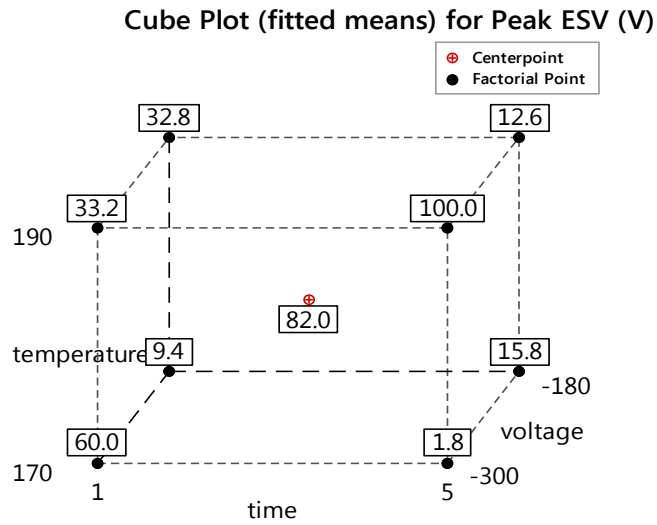


Figure 64. Positive potential ESV “cube” plot of the 2³ full factorial DOE given the effects of temperature (°C), time (hrs), and negative applied voltage (V) on the ESV (V). The average of the five peak ESV values for each wafer are shown at the corners and center of the plot.

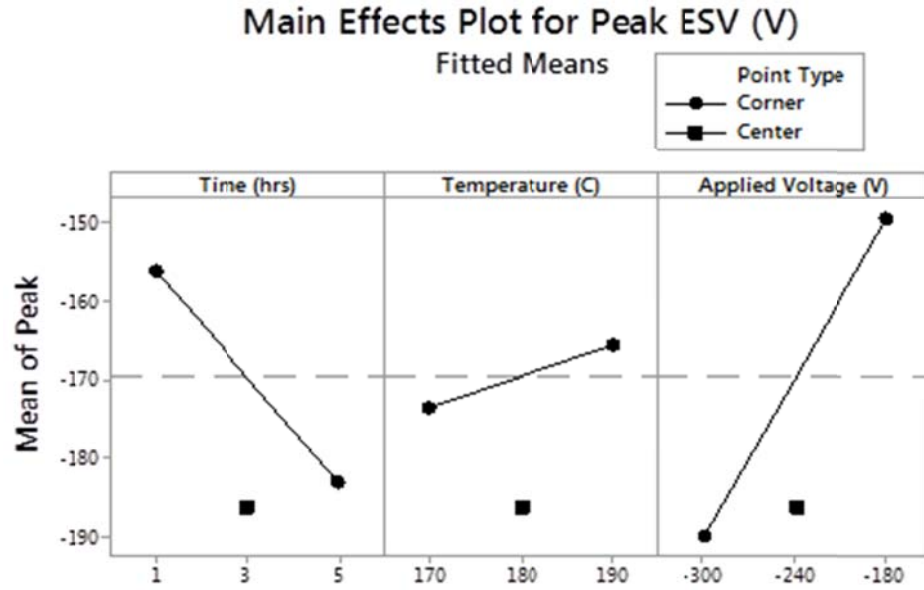


Figure 65. The “main effects” plot of the positive ESV as a function of temperature (°C), time (hrs), applied voltage (V).

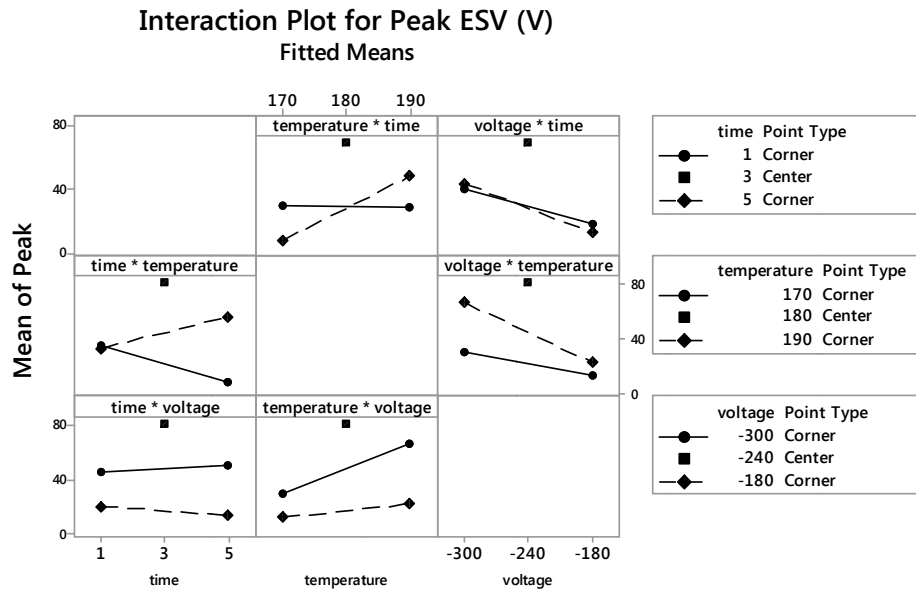


Figure 66. Positive potential ESV “interaction” plot of temperature (°C), time (hrs), and applied voltage (V).

4.3 Electret Characterization

Accelerated aging tests of the electrets were performed as described in Chapter III to determine the mean lifetime of the ESV for both positively and negatively activated wafers. The isothermal potential decay (ITPD) of the electret was evaluated over time while being maintained at a constant temperature of either 200°C, 250°C, 275°C, 300°C, 325°C. A sample was tested at each of the five ITPD temperatures from each of eight wafers. Four wafers were activated in the SUSS bonder for one hour at 170°C with an applied voltage of +300 V, while the four remaining wafers were activated for one hour at 170°C with an applied voltage of -300 V. The five point averaged maximum effective surface voltage produced for positive electret samples was 195.2 V, while the five point averaged maximum effective surface voltage produced for the negative electret samples was -194.2 V. Based on the calculations presented in section 2.6- “Effective Surface Voltage Electret Measurement” and Equation 13, the effective surface charge density is 4.0 mC/m² for both polarities, assuming the charge is at the silicon nitride-silicon oxide (blocking layer). This effective surface charge density is superior to the charge densities of organic electrets with parylene values the leading organic charge density reported as high as 3.7 mC/m² [103]. The ESV was found to decay exponentially for both the positive and negative ESV electrets. An example of the normalized ITPD data and fit curve is shown in Figure 67 and Figure 68 for samples from wafer 3. Comparison of the two figures show that the decay rate, τ , decreased for samples aged at higher temperatures. The decay rates were calculated by fitting

the measured ESV values to the best fit exponential decay equation as presented in Chapter III. The τ values for each sample of the eight wafers are presented in Table 6 for positive ESV samples and Table 7 for negative ESV samples. The decay rates of wafer 3 and wafer 4 of the positive ESV ITPD can be seen to have a significantly lower decay rate than wafer 1 and wafer 2 in the positive ESV study and significantly lower than all of the wafers in the negative ESV study. It is not clear why the range of decay rates for the positive ESV wafers is so broad. Figure 69 and Figure 70 provide plots of the exponential decay rate, τ , as an inverse function of temperature on a semi-log plot for positively charged and negatively charged electrets respectively.

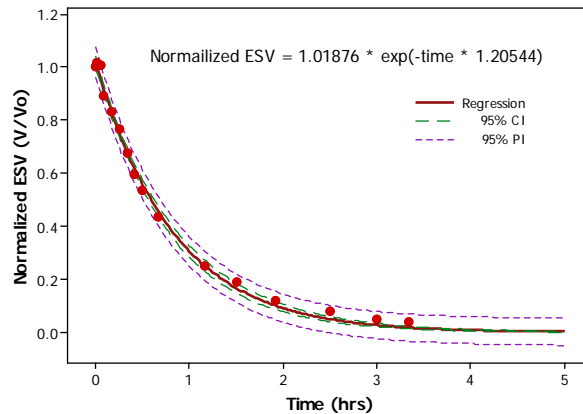


Figure 67. The ITPD plot for a sample from wafer 3 shows the ESV as a function of time, aged at 300°C. The sample was activated at 300 V for 1 hour at 170°C. The best fit regression to the exponential decay is provided with the 95% confidence interval and 95% prediction interval.

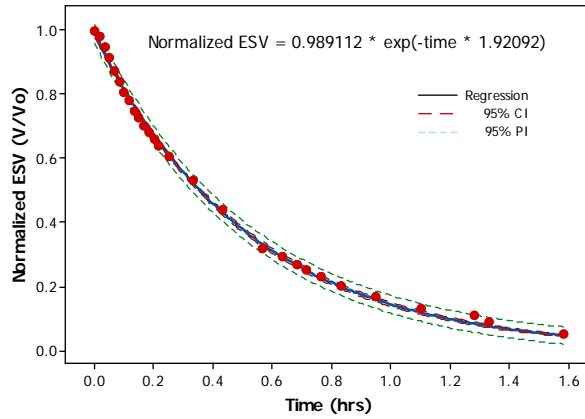


Figure 68. The ITPD plot for a sample from wafer 3 shows the ESV as a function of time, aged at 325°C. The sample was activated at 300 V for 1 hour at 170°C. The best fit regression to the exponential decay is provided with the 95% confidence interval and 95% prediction interval.

Table 6. Decay rates for positively charged electrets on four wafers at varying temperatures to predict the mean lifetime of the electrets.

Temperature (°C)	Wafer 1 τ (hrs)	Wafer 2 τ (hrs)	Wafer 3 τ (hrs)	Wafer 4 τ (hrs)	Average τ (hrs)	Std dev τ (hrs)
200	1036.80	943.40	392.20	518.10	722.63	273.16
250	30.81	47.38	36.06	24.15	34.60	8.50
275	6.27	10.70	7.03	5.11	7.28	2.09
300	1.79	2.67	0.83	3.32	2.15	0.94
325	0.35	0.30	0.52	0.98	0.54	0.27

Table 7. Decay rates for negatively charged electrets on four wafers at varying temperatures to predict the mean lifetime of the electrets.

Temperature (°C)	Wafer 1 τ (hrs)	Wafer 2 τ (hrs)	Wafer 3 τ (hrs)	Wafer 4 τ (hrs)	Average τ (hrs)	Std dev τ (hrs)
200	968.45	369.64	976.86	529.20	711.04	267.65
250	57.77	88.81	75.94	84.45	76.74	11.89
275	30.13	13.28	7.37	11.82	15.65	8.64
300	16.43	5.26	4.66	3.64	7.50	5.19
325	1.14	1.16	1.58	1.03	1.23	0.21

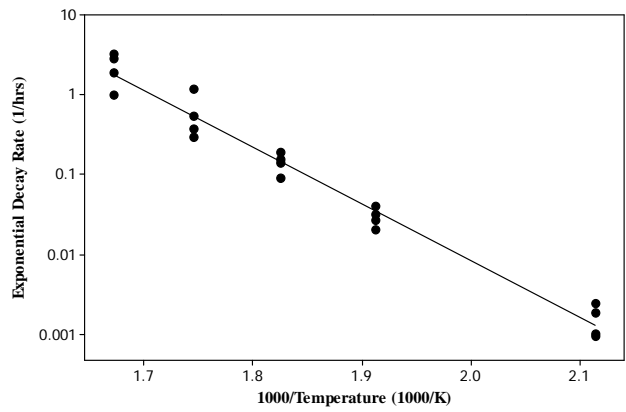


Figure 69. Positively charged electret, semi-log plot of the exponential decay rate vs 1000/Temperature. Samples from each of the 4 wafers were subjected to accelerated aging at 325°C, 300°C, 275°C, 250°C, and 200°C.

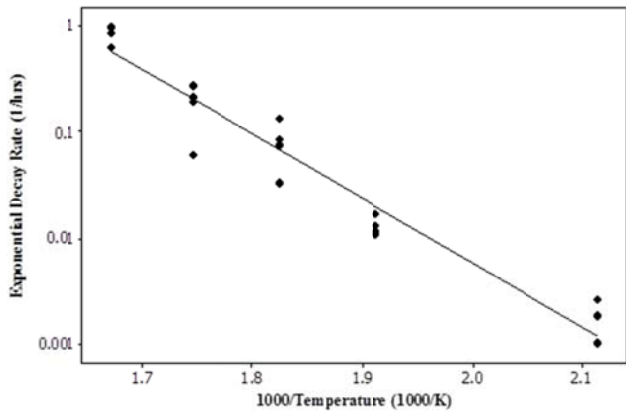


Figure 70. Negatively charged electret, semi-log plot of the exponential decay rate vs 1000/Temperature. Samples from each of the 4 wafers were subjected to accelerated aging at 325°C, 300°C, 275°C, 250°C, and 200°C.

Mean lifetime values for both positive and negative ESV were extrapolated for temperatures below the accelerated aging temperatures tested. These extrapolated

values are based on calculations of the activation energy for positive and negative ESV samples within the range of the accelerated aging temperature range. The calculated activation energy also provides insight and confirmation to the cause and location of the charge traps in the electret in conjunction with published values from other groups [55]. The best fit of the exponential decay constant for the positively charged electret is

$$\lambda(T) = 1.2869(10)^{12} e^{\frac{-1.4067}{kT}}. \quad \text{Equation 37}$$

The activation energy of the positive electret is 1.41 eV. The coefficient of determination (R-sq) for the exponential decay rate of the positive electret is 97.3%. The best fit of the exponential decay constant for the negatively charged electret is

$$\lambda(T) = 8.356(10)^9 e^{\frac{-1.2037}{kT}}. \quad \text{Equation 38}$$

The activation energy of the negative electret is 1.20 eV. The coefficient of determination for the exponential decay rate of the negative electret is 94.8%. The isothermal potential decay of the electret is extrapolated by evaluating Equation 37 and Equation 38 at a temperature of 125°C. The positive electret has a mean lifetime value of 57.7 years, while the mean lifetime value of the negative electret was 23.9 years if maintained in an environment at 125°C. The rate of decay for this multilayer electret is 5 times slower than the elevated temperature rate of decay for PECVD electret layers produced by other groups [2, 51].

Stoichiometric Si_3N_4 produce traps with activation energy levels of 1.4 eV, while energy level of traps in silicon rich LPCVD silicon nitride have been measured by other groups to be in the 0.80 eV range [55]. The experimentally determined activation energy requirements of the multilayer PECVD oxide/nitride film were 1.41 eV and 1.20 eV for positive electrets and negative electrets respectively. The values appear reasonable given the documented effects of a high hydrogen content for our PECVD silicon nitride film and, the unquantified effects that the nitride is only part of a multilayer stack with PECVD silicon oxide layers.

4.4 Application of Electret as an Electrochemical Etch Stop

After successfully fabricating the electrets, it was desired to explore new applications that would benefit from the implementation of the electret. In particular, this study explored the use of the electret as part of an electrochemical etch stop in the anisotropic etching of silicon with TMAH. The electret was used as a replacement for an external bias typically used in a MIS etch stop process. This type of bias has been supplied in MIS and p-n junction electrochemical etch stop techniques in the form of external electrodes, as presented in the background of section 3.6 – “Application of Electret as an Electrochemical Etch Stop”. Without this bias, chemical etching in the [100] silicon direction would continue unabated. A model of the etch band diagram for the implemented etch is shown in Figure 71. With the bias, a depletion region is produced and the anodic partial current that is generated during etching between the substrate and electrolyte are eliminated,

bringing the etching process to a stop in proximity to the depletion region [19, 98, 99].

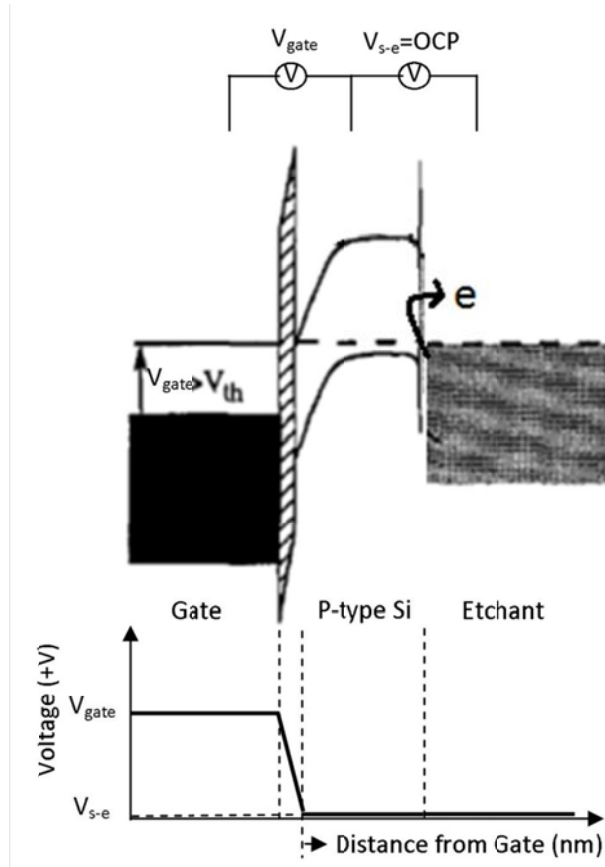


Figure 71. A band diagram of a the MIS etch stop with bias between gate and silicon and in open circuit potential between the silicon and electrolyte, alkali based etchant, showing the drift of electrons into the electrolyte and continuing the etch process with hydroxyl ion generation. The figure is modified from Smith and Soderbarg 1993 [19].

The raw data of the average etch depth measurements from the electrochemical etch study outlined in section 3.6.4 - "Electrochemical Etch Stop Timed Study

Overview” is presented in Figure 72 with the data provided in Table 8, Table 9, and Table 10. The mean final silicon etch rate of the positive electret samples was 11.9 $\mu\text{m/hr}$ while the mean final silicon etch rate for neutral and negative electret samples were 8.6 $\mu\text{m/hr}$ and 8.8 $\mu\text{m/hr}$ respectively. The initial ESV of each respective sample is present at the bottom of the table. Additional qualitative ESV measurements were taken of the samples in trial 3 with the samples loaded into the etch cells. During the etch stop experiments for trial 1 and 2, one question that was raised was the integrity of the electret during the etching process. Specifically, preliminary studies indicated that when the electret came into contact with a fluid, the electret is neutralized. Thus, in trial 3, the experimental protocol was changed to include the measurement of the electret while mounted in the etch cell to confirm that the electret was maintained throughout the etching process. The qualitative measurements were made before etching and once the etching process was completed with the intention of confirming that the integrity of the electret charge was maintained throughout the etching process. The results of these measurements, Table 11, show that 67% of the samples maintained a significant portion of their ESV even once the etchant had etched through the silicon to PECVD multilayer film in the cavity regions of the substrate. This is an acceptable yield considering the large removal of material and the masking of charge possible due to etch solution in direct contact with the back side of electret.

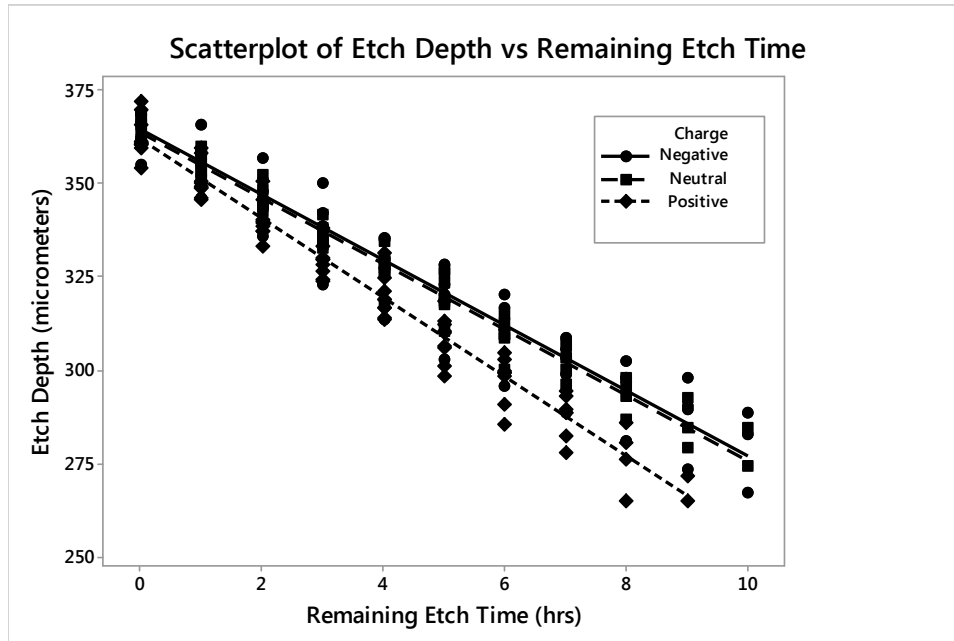


Figure 72. A linear best fit for etch depth samples as a function of the time remaining to the end of the silicon etch are grouped by electret potentials; positive, negative, and neutral.

Table 8. Trial 1 etch depth vs time for neutral, negative, and positive electrets.

Trial 1	Neutral			Negative			Positive		
	Die 1	Die 2*	Die 3	Die 1	Die 2	Die 3	Die 1	Die 2	Die 3
Time (hr)	Etch Depth (microns)								
0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
18	300.3	330.7	284.7	239.9	289.3	335.4	293.2	264.8	318.4
19	310.5		292.8	250.3	298.0	350.4	304.5	276.0	331.4
20	318.0		297.9	257.1	303.2	357.0	312.4	282.4	338.2
21	332.7		307.1	267.3	311.0	365.8	324.7	290.9	350.8
22	342.6		314.9	273.2	320.2	368.6	333.5	301.0	359.6
23	358.1		327.2	281.1	330.1		346.0	313.6	372.0
24	368.0		334.7	288.6	338.5		358.2	323.7	
25			342.0	295.9	348.3		370.2	337.1	
26			352.5	302.8	357.8			349.0	
27			360.3	313.7	369.6			365.9	
28			366.0	323.1					
29				336.2					
30				346.2					
31				355.1					
32				368.7					
ESV (V)	0	0	0	-150	-250	-150	150	150	250

* Die 2 of the neutral die set fractured in the etch cell.

Table 9. Trial 2 etch depth vs time for neutral, negative, and positive electrets.

Trial 2	Neutral			Negative			Positive		
	Die 1	Die 2	Die 3*	Die 1	Die 2	Die 3	Die 1	Die 2	Die 3
Time (hr)	Etch Depth (microns)								
0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
18	274.2	284.7	288.9	206.8	208.9	217.0	289.3	264.7	271.6
19	279.1	293.0					299.5	277.8	280.6
20	286.9	300.0					306.0	285.2	288.7
21	296.1	309.6					316.9	298.5	299.7
22	308.5	326.2	323.5				328.3	314.2	309.8
23	317.4	329.6	328.2				338.7	324.4	318.9
24	326.8	338.2	336.0				349.4	337.5	329.8
25	335.3	348.6	344.0				360.5	346.1	339.6
26	345.0	358.6	352.9					359.6	350.3
27	353.6	367.8	361.4						361.5
28	364.5								
ESV (V)	0	0	0	-150	-225	-150	175	150	250

* Die 3 of the neutral die set fractured in the etch cell and was replaced with a neutral die from an extra wafer.

Table 10. Trial 3 etch depth vs time for neutral, negative, and positive electrets.

Trial 3	Neutral			Negative			Positive		
	Die 1*	Die 2	Die 3	Die 1	Die 2	Die 3	Die 1	Die 2	Die 3
Time (hr)	Etch Depth (μm)								
0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
18	223.9	312.5	295.7	282.8	298.9	288.4	288.5	299.5	285.7
19		319.4	303.3	290.2	310.9	297.9	298.4	310.3	294.3
20		327.6	309.6	297.9	318.8	302.7	306.6	319.1	302.8
21		334.7	318.4	305.7	327.4	308.7	316.7	329.9	313.0
22		344.9	326.3	316.9	338.7	320.4	326.7	340.2	321.4
23		351.4	333.9	323.1	345.6	328.5	333.3	348.8	330.0
24		361.4	344.7	329.9	358.7	335.0	345.9	360.9	340.7
25			355.5	337.3	369.6	342.4	354.3		350.5
26			361.8	346.5		351.0			360.7
27				355.4		358.7			
28				361.6		366.4			
ESV (V)	0	0	0	-150	-160	-150	160	170	150

* Die 1 of the neutral die set fractured in the etch cell.

Table 11. ESV measurements for etch test die in trial 3.

		Die ESV (V)	Die in Etch Cell	
			Initial ESV (V)	Final ESV (V)
Neutral	Die 1	0	0	0
	Die 2	0	0	0
	Die 3	0	0	0
Negative	Die 1	-150	-65	-20
	Die 2	-160	-110	-80
	Die 3	-150	-92	0
Positive	Die 1	160	133	100
	Die 2	170	123	98
	Die 3	150	47	0

A one-way ANOVA was performed to determine if there a significant difference in the etch rate between the electret, positive, neutral, and negative ESV groups in the last stages of etching before reaching the electret. The final etch rate was determined by taking the difference between the final etch depth measurement and the prior etch depth measurement. The mean value of the final etch rate for the positive ESV electret is 11.9 $\mu\text{m/hr}$ verses the mean value of the final etch rate for neutral and negative ESV electrets of 8.6 $\mu\text{m/hr}$ and 8.8 $\mu\text{m/hr}$ respectively, Table 12. The “Null Hypothesis” is that there is no statistical difference in the final etch rate between samples grouped by electret potential. The null hypothesis is tested by evaluating the P-Values of the final etch rates grouped by charge with 3 separate 2 sample T-test using MINITAB. The P-value, which represents the probability of obtaining repeated differences between groups of data, is presented for the final etch rate between positive-neutral, negative-neutral, and negative-positive ESV groups, Table 13. By “null hypothesis”, no significant difference in etch rate was

identified between the negatively charged electret and neutral samples; the P-value of the ANOVA between the two sample groups was over 0.90. However, the final etch rate of silicon for the positive electret was found to be significantly different than both the neutral and negative electrets. The P-value for the ANOVA between the positive electret and neutral samples was less than 0.01 and the P-value between the positive electret and neutral electret was 0.07. As a final analysis of the null hypothesis, all three of the charge groups were compared simultaneously using an ANOVA with a resulting P-value of 0.042 and a resulting strong significance to the rejection of the null hypothesis.

Table 12. Final silicon etch rate grouped by neutral, negative, and positive ESV electret.

	Final Etch Rate ($\mu\text{m/hr}$)	
	Mean	Standard Deviation
Neutral	8.6	1.9
Negative	8.8	3.9
Positive	11.9	2.3

Table 13. Null Hypothesis P Values for the Final Etch Rate with 3 separate 2 sample T-test using MINITAB

P Value	Neutral	Positive
Positive	0.009	-
Negative	0.903	0.073

As indicated in the raw data, and confirmed by “null hypothesis” tests, a surge in etch rate occurred at the end of the etching process for the positively charged electrets. One possible explanation for this behavior is that there was an increase in

electrons available in the silicon at the silicon-electret interface due to the strong inversion of the gate bias. This abundance of electrons in the p-type silicon provided a “stock” of electrons available to the electrolyte interface as the silicon layer thins; thereby, adjusting the Fermi level in accordance to the changing open circuit potential OCP. The extra supply of electrons diffused to the silicon-electrolyte interface as a minority carrier and was injected into the electrolyte producing a short term increase in OH⁻ groups and silicon etching [19]. This is a behavior similar to the etch rate one would see in a cathodically biased silicon etch in a base solution [104].

It is customary to run an electrochemical etch stop with a controlled positive potential applied between the silicon substrate and the electrolyte. With this positive bias, electrons are drawn to the silicon-gate interface and away from the electrolyte, breaking the etch cycle which requires a continuous supply of hydroxyl ions for silicon to etch [19]. Without this bias between the substrate and electrolyte, Figure 71, the free electrons that are generated during the etch process return to the analyte and reduce the water producing additional hydroxyl ions for silicon etching and hydrogen gas as a byproduct. At most, with no applied bias between the silicon and electrolyte, a transient etch rate response can be expected due to the electric field produced by the electret. It is reasonable that the positively charged electret elicits a faster etch rate than the neutral and negative electret in the final stage of the silicon etching. A sole positive bias of the gate in the MIS etch stop provides a

rich source of electrons as the silicon at the interface of the gate is in strong inversion and past the threshold voltage, V_{th} . [19].

5 CONCLUSIONS

The electret activation process for a thin multilayer $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ PECVD film has been optimized using a silicon wafer as the contact electrode in a thermally assisted poling process. Effective surface voltages in excess of -225 V were produced with cathodic contact using processes and equipment standard to microfabrication facilities. The optimum process for maximizing the negative ESV was determined to be five hours at 170°C with an applied voltage of -540 V with the SUSS SB-6e. The maximum five point averaged ESV produced for positive electret samples was 195.2 V, while the maximum five point averaged ESV produced for the negative electret samples was -194.2 V. The act of single polarity charging produced regions of positively and negatively charged electret where the regions in direct contact with the silicon contact electrode during the activation step developed an ESV complementary to the polarization of the electrode. On the other hand, regions not in direct contact developed a charged ESV opposite to the polarization of the electrode during activation. Longer activation periods resulted in larger complementing and opposing ESV values.

Characterization of the films by isothermal potential decay show that the inorganic positive electret has an extrapolated mean lifetime value of 57.7 years; while the extrapolated mean lifetime value of the negative electret was 23.9 years at

a continuous temperature of 125°C. Thermal neutralization of the electret through isothermal potential decay studies demonstrated an activation energy of 1.4 eV and 1.2 eV for the positive electrets and negative electrets, respectively.

When using the electret as a MOS biased etch stop, the data demonstrated the positively charged electret produced a statistically significant increase in etch rate, when compared to the neutral and negatively charged electrets. However, overall the MOS bias caused by the electret did not produce a definitive etch stop for the configuration presented in this study. These results suggest that, to act as an etch stop, a positive bias must be maintained on the silicon wafer with respect to the etchant.

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CURRICULUM VITAE

MARK CRAIN

PROFESSIONAL EXPERIENCE

Research Engineer/Graduate Teaching Assistant---University of Louisville, 2011-Present

- Completing Ph.D. in Electrical Engineering under the support of the Bioengineering Department “The Development of Multilayer Thin Film Electrets for Microfabrication Processing”
- Microfabrication Specialist for “Optical and Electrical Phytoplankton Detection, Size, and Count Flow Cytometry On a Chip”

Cleanroom Manager/Research Engineer---University of Louisville, 1999-2011

- Developed the University of Louisville MicroNano Technology Center to provide basic microfabrication services to Universities, government and industry-- both local and international.
- Managed 4 technical staff, 2 administrative staff, and 3-5 student work studies.
- Team member for the design and installation of the new cleanroom facility located in the University of Louisville Belknap Research Building
- Produced numerous contributions in the development of microfabrication technology for grant funded research. Areas of extensive research experience include capillary electrophoresis, capacitive pressure transducers, thermal and optical microphones, chemical pre-concentrators, and radiation detectors.
- Managed capital equipment selections, purchases, and installations. Committee member determining equipment needs. Managed “Requests for Proposals” from equipment vendors. Managed commissioning and installation terms and acceptance testing.
- Operated an active outreach program, brought many thousands of young students (K-12) through the cleanroom providing interactive tours.
- Developed and implemented safety protocols with the support of University Health and Safety.
- Developed significant project relationships with NSWC Crane, Zyvex, and MPD, Inc.

- Cleanroom manager on organization committee for the University, Government, and Industry Micro/nano Symposium held at the University of Louisville 2008 and showcasing our new facility.
- On search committee for the University of Louisville Vice-President for Research and Industry 2010

Graduate Research Assistant---University of Louisville, 1997- 1999

- Designed and implemented of a student laboratory course for the fabrication and testing of a microfabricated piezoresistive pressure transducer.
- Developed of many microfabrication processes, the production of corresponding SOPs, training students and research staff, ordering supplies, and maintaining research equipment.
- Instructor of the U of L Microfabrication Laboratory Course (1997-2003).

Project Manager---North American Stainless (New Installation Department), 1993-1996

- Developed written equipment specifications; prepared bid packages and contracts; supervised the start-up and installation of new process lines and support equipment.
- Responsible for major installation projects including a cold rolling mill, multiple finishing lines and mill duty overhead cranes (over \$50M in equipment).

Laboratory Manager North American Stainless (Quality-Control Department), 1991-1993

- Coordinated the design and construction of the product certification laboratory during plant start-up.
- Responsible for purchasing laboratory equipment, hiring and training laboratory personnel; and creating SOPs required for certification and evaluation of mechanical and metallurgical properties of processed stainless steel in accordance with ASTM, ISO 9000, and specific industry standards.

EDUCATION

University of Louisville, Louisville, KY

Completing Electrical Engineering Doctor of Philosophy (Ph.D) degree, Fall 2014

MS in Electrical Engineering (MSEE), August 1999

Purdue University, West Lafayette, IN

BS in Mechanical Engineering (BSME), May 1991

REFEREED JOURNAL PUBLICATIONS

- R. S. Pai, M. M. Crain, and K. M. Walsh, "Maskless shaping of gold stud bumps as high aspect ratio microstructures," *Microelectronic Engineering*, vol. 88, pp. 135-139, Jan 2011.
- R. S. Pai, K. M. Walsh, M. M. Crain, T. J. Roussel, D. J. Jackson, R. P. Baldwin, *et al.*, "Fully Integrated Three-Dimensional Electrodes for Electrochemical Detection in Microchips: Fabrication, Characterization, and Applications," *Analytical Chemistry*, vol. 81, pp. 4762-4769, Jun 15, 2009.
- S. Carroll, R. P. Baldman, M. M. Crain, and K. Walsh, "ANYL 195-Room temperature UV adhesive bonding of CE devices," *Abstracts of Papers of the American Chemical Society*, vol. 235, Apr 6 2008.
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- J. T. Lin, K. W. Walsh, D. Jackson, J. Aebbersold, M. Crain, J. F. Naber, *et al.*, "Development of capacitive pure bending strain sensor for wireless spinal fusion monitoring," *Sensors and Actuators a-Physical*, vol. 138, pp. 276-287, Aug 26 2007.
- M. Martin, M. Crain, K. Walsh, R. A. McGill, E. Houser, J. Stepnowski, *et al.*, "Microfabricated vapor preconcentrator for portable ion mobility spectroscopy," *Sensors and Actuators B-Chemical*, vol. 126, pp. 447-454, Oct 1 2007.
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- D. J. Jackson, J. F. Naber, T. J. Roussel, M. M. Crain, K. M. Walsh, R. S. Keynton, *et al.*, "Portable high-voltage power supply and electrochemical detection circuits for microchip capillary electrophoresis," *Analytical Chemistry*, vol. 75, pp. 3643-3649, Jul 15 2003.
- R. P. Baldwin, T. J. Roussel, M. M. Crain, V. Bathlagunda, D. J. Jackson, J. Gullapalli, *et al.*, "Fully integrated on-chip electrochemical detection for

- capillary electrophoresis in a microfabricated device," *Analytical Chemistry*, vol. 74, pp. 3690-3697, Aug 1 2002.
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 - W. K. Pitts, M. D. Martin, S. Belolipetskiy, M. Crain, J. B. Hutchins, S. Matos, K. M. Walsh, K. Solberg, "Development and Operation of Laser Machined Microwell Detectors", *Nuclear Instruments and Methods in Physics Research A* 438 (1999) 277-281
 - R. W. Cohn, S. F. Lyuksyutov, K. M. Walsh, and M. M. Crain, "Nanolithography considerations for multi-passband grating filters," *Optical Review*, vol. 6, pp. 345-354, Jul-Aug 1999.
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