12-2017

Control of power electronic interfaces in distributed generation.

Mohammad Mohebbi
University of Louisville

CONTROL OF POWER ELECTRONIC INTERFACES IN DISTRIBUTED GENERATION

By

Mohammad Mohebbi
B.Sc. Electrical Engineering, Amirkabir Univ. of Tech.
M.Sc. Electrical Engineering, Iran Univ. of Sci. & Tech.

A Dissertation
Submitted to the Faculty of the
J.B. Speed School of Engineering of the University of Louisville
in Partial Fulfillment of the Requirements
for the Degree of

Doctor of Philosophy in Electrical Engineering

Department of Electrical and Computer Engineering
University of Louisville
Louisville, Kentucky

December 2017

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Mohammad Mohebbi

B.Sc. Electrical Engineering, Amirkabir Univ. of Tech.

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A Dissertation Approved On

October 23, 2017

by the following Dissertation Committee:

Michael McIntyre (Dissertation Director)

Tamer Inanc

John Naber

Chris Richards

DEDICATION

This dissertation is dedicated to my wife, Nadieh, who has been a constant source of support and encouragement during the challenges of my journey of Ph.D. and life. I am truly thankful for having you in my life. This work is also dedicated to my parents who have always loved me unconditionally.

I dedicate this work and give special thanks to my parent-in-law who never left my side. This work is also dedicated to my wonderful daughter, Nikki. I love you to the moon and back.

ACKNOWLEDGEMENTS

This work would not have been possible without the help of many people. I would like to express my deepest gratitude to my advisor, Dr. Michael McIntyre, for his excellent guidance, advice, caring, and for giving me so many wonderful opportunities.

Similar, profound gratitude goes to Dr. John Naber, a member of my dissertation committee for his great help and strong support. I have had the pleasure to work with Dr. Naber and his research group during this and other related projects.

I extend my thanks to the rest of my committee members, Dr. Tamer Inanc and Dr. Chris Richards. Each of the members of my dissertation committee has provided me extensive professional guidance and helpful suggestions.

I would like to thank Joseph Latham, who as a good friend, was always willing to help and give his best suggestions. It would have been a lonely lab without him.

ABSTRACT

CONTROL OF POWER ELECTRONIC INTERFACES IN DISTRIBUTED GENERATION

Mohammad Mohebbi

October 23, 2017

Renewable energy has gained popularity as an alternative resource for electric power generation. As such, Distributed Generation (DG) is expected to open new horizons to electric power generation. Most renewable energy sources cannot be connected to the load directly. Integration of the renewable energy sources with the load has brought new challenges in terms of the system's stability, voltage regulation and power quality issues. For example, the output power, voltage and frequency of an example wind turbine depend on the wind speed, which fluctuate over time and cannot be forecasted accurately. At the same time, the nonlinearity of residential electrical load is steadily increasing with the growing use of devices with rectifiers at their front end. This nonlinearity of the load deviates both current and voltage waveforms in the distribution feeder from their sinusoidal shape, hence increasing the Total Harmonics Distortions (THD) and polluting the grid. Advances in Power Electronic Interfaces (PEI) have increased the viability of DG systems and enhanced controllability and power transfer capability. Power electronic converter as

an interface between energy sources and the grid/load has a higher degree of controllability compared to electrical machine used as the generator. This controllability can be used to not only overcome the aforementioned shortfalls of integration of renewable energy with the grid/load but also to reduce THD and improve the power quality. As a consequence, design of a sophisticated controller that can take advantage of this controllability provided by PEIs to facilitate the integration of DG with the load and generate high quality power has become of great interest. In this study a set of nonlinear controllers and observers are proposed for the control of PEIs with different DG technologies. Lyapunov stability analysis, simulation and experimental results are used to validate the effectiveness of the proposed control solution in terms of tracking objective and meeting the THD requirements of IEEE 519 and EN 50160 standards for US and European power systems, respectively.

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CHAPTER 1

INTRODUCTION AND MOTIVATION

As Distributed Generation (DG) systems [1]-[2][3] [4], Vehicle to Grid (V2G) [5], Battery Energy Storage System (BESS) [6] and Uninterruptable Power Supplies (UPS) [7]-[8][9][10] are more widely adopted, pulse width modulated (PWM) power converters have become more broadly utilized for voltage conversion. Among a wide variety of structures proposed for the PWM power converters, those composed of a switching circuit followed by an output LC filter have gain more popularity for the DC:DC power converters and DC:AC standalone voltage source inverters (VSI) [1]- [10]. Fig. 1.1 demonstrate a general class of PWM converters consisting of a PWM switching circuit followed by an output *LC* filter. This class of PWM covertures includes a wide variety of both dc-dc and dc-ac converters such as buck, synchronous buck, forward, push-pull, full and half-bridge converters and inverters with output *LC* filter. All the converters/ inverters in this class can be considered as derivatives of the basic buck converter. Because of the same dynamic model for all the converter/inverter in this class, any controller developed for each is applicable for others as well.

As shown in Fig 1.2, a power inverters have two operation modes: stand-alone and grid-tie. In stand-alone mode, the local load is supplied by the inverter. Therefore, generation of a high-quality output voltage with low distortion and excellent voltage

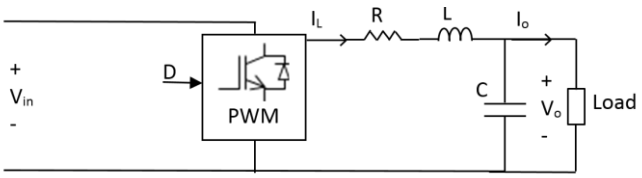

Fig. 1.1 Buck-type converter.

regulation as well as disturbance rejection are the essential requirements of the associated control system. Good transient response and insensitivity to the load and system parameter variations are other metrics in the performance evaluation of inverters, which also necessitates the use of high performance controllers. In grid-tie mode, the inverter is controlled as a current source. The grid-tie inverters, known as grid-feeding power converters, can participate in the control of the grid voltage amplitude and frequency by adjusting, in a higher level control layer, the references of their active and reactive power. In a lower level control layer, the local controller is responsible to keep the active and reactive power generated by the inverter as close as possible to their reference values.

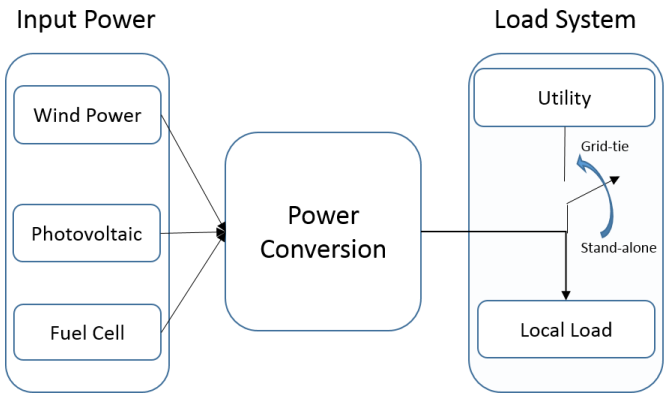

Fig. 1.2 General structure for DG

Many control techniques such as proportional–resonant (PR) [11], [12], multiloop feedback control [13]-[14] [15] dead-beat control [16] and repetitive control [17]-

[18][19][20][21][22][23][24] have been proposed to control a single phase VSI in standalone mode. Although a single output voltage measurement is sufficient for the control of the inverter, to the best knowledge of the authors, the majority of the existing control approaches require an inductor current measurement. Using two measurements gives these controllers improved system stability and dynamic performance through both output voltage and inductor current regulation. For example, a simple multiloop control technique utilizes two traditional Proportional, Integral, and Derivative (PID) controllers to regulate both output voltage and inductor current in the voltage and current control loops, respectively. Finite loop gain of the PID controller at the fundamental frequency and its sensitivity to the load variations have motivated combining other techniques such as frame transformation [25]-[26][27] and Load Current Feedback (LCF) [14], [28], [29] to the multiloop control scheme. These combinations alleviate shortfalls of the multiloop control scheme at the cost of more computational complexity resulting from signal transformations between frames and an extra current sensor for an output current measurement.

Repetitive control is known for its capability to overcome periodic disturbances, whose frequencies are less than half of the sampling frequency [17]- [24]. However, slow dynamics and poor tracking performance especially to nonperiodic disturbances are the main practical limitations of this technique. A multi-resonant harmonic compensator which eliminates low-order load current harmonics and periodic disturbances with specific frequencies has been applied to inverter control as shown in [30]-[31][32][33] [34]. Lack of a systematic method of stabilization is a general problem for both repetitive and resonant regulator control schemes [35]. In [36] a Fuzzy control strategy was used to control the inverter system, with a genetic algorithm used in conjunction to optimize the fuzzy

controller. The scheme presented in [36] has an acceptable dynamic response and output voltage waveform at the cost of a complex algorithm.

Nonlinear control techniques such as backstepping controller and sliding mode control have been shown to demonstrate good tracking performance. Discrete-time sliding mode control technique has been used in multi-loop feedback systems due to its overshoot-free tracking capability [37]. However, the dependency of these controllers to the knowledge of the system parameters limits their practical application. In [38] the performance of two nonlinear controllers, namely backstepping and sliding mode controllers, are compared with a conventional PID controller. The results show the backstepping controller outperforming the other two controllers. The sliding mode controller always generates a very harsh command compared to backstepping [38]. The control laws of the proposed backstepping and sliding mode controllers in [38] depend on the numerical derivative of the output current which increase the level of the noise in the system.

In the majority of the control schemes presented for the control of power converters with output LC filter, at least two sensors are used to measure the output voltage and the inductor current. In practice this inductor current measurement has a significant amount of ripple and measurement noise resulting from the switching scheme. This noise and ripple are then propagated into the control algorithm adding noise and disturbance to the system. Some control schemes use capacitor current measurement instead of the inductor current measurement [8], [14], [39]- [40] [41] where the same problem remains. Also some works use an output current sensor in addition to the other two sensors [14], [26], [39] to reduce the effect of the high frequency noise and ripple resulting from switching, utilization of a low-pass filter (LPF) is suggested. Addition of LPF introduces phase delays, which can

have an adverse effect on the control schemes, which can limit any performance improvement.

In this dissertation, nonlinear control techniques such as backstepping controller and filter-based controller are utilized for the control of power converters in different applications of DG systems. To overcome the shortfalls of the backstepping controller such as dependency of the control law to the inductor current measurement and numerical derivative of the noisy current measurement, as seen in [38], a combination of the backstepping controller with other control techniques such as inductor current observer, output current observer, nonlinear sliding technique and periodic learning is proposed. Also, filter-based control techniques are developed as effective control schemes which require only single output voltage measurement in their control law. The proposed filter-based control schemes not only eliminate the need for costly current sensors to measure the inductor and/or output currents, but also they are robust against system parameter discrepancy and system disturbances. For each developed control scheme, a Lyapunov stability analysis is presented which proves that the voltage tracking objective is achieved by the controller with all signals remaining bounded. Simulation and/or experimental results further validate the proposed approaches.

The rest of the dissertation is organized as follows. In Chapter 2, a backstepping controller is utilized to control a two-stage PEI in the V2G application. The proposed controller in this chapter is combined with sliding technique to compensate for the uncertainty presented by the derivative of the output current presence in the model. An energy efficient two-stage DC to AC PEI is presented in Chapter 3. A typical DC:AC conversion system consists of two stages, a DC:DC converter to generate the necessary bus

voltage followed by an inverter which generates the desired AC output. A modification of this system is proposed for the purpose of reducing switching losses. The proposed two-stage system consists of a buck converter which produces a mixed (DC+AC) signal which is fed to an H-Bridge inverter. This mixed signal is designed such that it reduces the switching loss across the inverter switches while still providing the necessary voltage for the inverter input. Backstepping controllers are designed to achieve output voltage tracking objectives for both stages. In Chapter 4, a nonlinear backstepping controller combined with a periodic disturbance learning observer is proposed for the control of a single-phase H-Bridge inverter under both linear and nonlinear loads. The proposed learning scheme takes into account the periodic nature of the system and observes the periodic disturbance and unmeasurable uncertainties of the system. Chapter 5 details an extension of the proposed control techniques for the control of a 3-phase 4-wire diode clamped inverter with an output LC filter under different loads including balanced, unbalanced, linear and nonlinear loads. Also, the seamless transition of inverter from standalone to grid-tie is investigated while the inverter is under the control of the proposed controller. Furthermore, a load-current observer is combined with the proposed backstepping controller to enhance the behavior of the controller.

As an effort to remove the inductor current measurement from the control law, an inductor current observer is developed and combined with a backstepping controller in Chapter 6. The elimination of the sensor along with the removal of current ripple and noise from the control algorithm provides an advantage over existing arts in this area. To further improve the performance of the control law and make it robust against system parameters discrepancies and compensate for system disturbances, in Chapter 7, 8 and 9 filter-based

control approach is investigated. This control technique inherently benefits from an internal observer so that its control law is only relying on the system output and it doesn't need extra measurement for the other system states. The basic form of the proposed filter-based controller is presented in Chapter 7. The control law of the proposed filter-based controller relies only on the output voltage measurement which eliminate the need for costly current sensors to measure the inductor and/or output currents. Also, a disturbance observer is combined to the developed control scheme which makes it more suitable for practical purposes and compensates for an unknown disturbance in the model. Various system uncertainty including dead-time in modulation scheme, voltage drop across switching devices and input voltage deviations are compensated with this unknown disturbance observer. To reduce the control sensitivity to the system parameters and compensate for parameter variation, two extension of the filter-based control scheme are presented in Chapter 8 and 9. In the earlier scheme, presented in Chapter 8, the control law is developed for unknown system parameters whereas in the later scheme, presented in Chapter 9, the nominal values of the system parameters are utilized and the control scheme compensates for parameter discrepancies. Finally, conclusions and suggested future work are given in Chapter 10.

CHAPTER 2

VEHICLE TO GRID UTILIZING A BACKSTEPPING CONTROLLER FOR BIDIRECTIONAL FULL-BRIDGE CONVERTER

With environmental and climate change issues, increasing oil prices, concerns about energy security, decreasing fossil energy reserves, and environmental related legislation, plug-in electric and hybrid vehicles (PEVs) sales are increasing. Meanwhile with "vehicle to grid" (V2G) technology, electric vehicles can work as distributed resources and power can be sent back to the utility. This fact places V2G as an emerging technology with the potential to revolutionize the electric power industry [42]. V2G technology utilizes the energy stored in a battery electric vehicle (BEV) or plug-in hybrid electric vehicle (PHEV) for connection to the grid. This technology can be used in conjunction with a Smart Grid or as a supplemental/backup power source for a household [5]. One such application is the use of a V2G interface to power a household entirely from the vehicle's battery. This system would replace the need for a large backup generator and add the convenience of a more portable system located in the user's vehicle. The main objective of this system is to produce a sufficient, sustained power source.

A V2G system typically consists of a two-stage power electronic interface (PEI). The first PEI stage is a DC:DC converter which steps up/down the voltage of the EV's battery

pack to the bus voltage necessary for the second PEI stage, the inverter. The inverter converts this DC bus voltage to an AC voltage compatible with that of the grid. This work focuses on the design and control scheme of the DC:DC converter stage of the V2G system [43]. A robust design for this PEI necessitates the ability to adapt to a varying input voltage and an unknown load while still maintaining the desired output voltage. As such, a backstepping controller is ideal because of its adaptive nature. Development of such a controller is presented herein as designed for a full-bridge DC:DC converter. The second PEI stage of the design is implemented via two parallel ANPC inverters with 180° phase difference providing a fixed magnitude, fixed frequency split-phase AC voltage.

2.1 V2G system Design

The proposed two-stage V2G system is shown in Fig. 2.1. As shown the first PEI stage is designed to convert the 240 [V] DC voltage of the battery pack to the 340 [V] DC bus voltage necessary for inversion. The second PEI stage consists of two five-level ANPC inverters which convert the 340 [V] bus voltage to a 240 [V_{rms}], 60 [Hz] split-phase AC voltage. In the subsequent section, the bidirectional full-bridge converter and the related controller are designed to meet the requirements set by the second stage inverters.

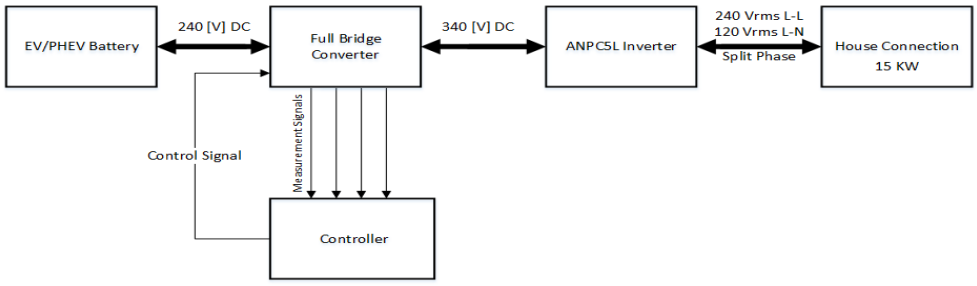

Fig. 2.1 System Block Diagram for Generating 240 [V_{rms}] Split-Phase AC Voltage from 240V DC Input.

2.1.1 Five-Level ANPC Inverter

Two parallel five-level ANPC (ANPC5L) converters with 180° phase difference, shown in Fig. 2.2, are capable of generating a five-level 120 [V_{rms}] line-to-neutral output voltage and nine level 240[V_{rms}] line-to-line split-phase AC voltage which fulfills the harmonic limits of the IEEE519 standard when a simple LC filter is applied.

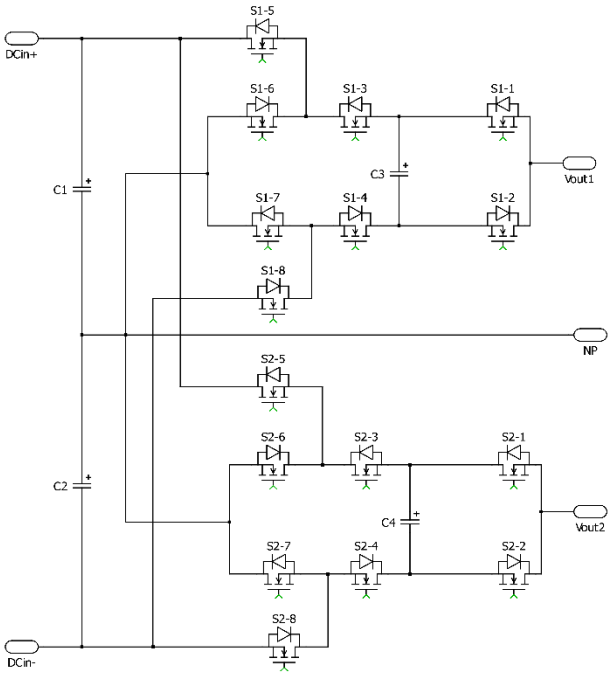

Fig. 2.2 Two parallel five-level simplified ANPC with 180° phase difference.

In order to reduce the cost and size of the inverter, a simplified ANPC5L topology was chosen which requires only one floating capacitor. The voltage of this floating capacitor is controlled based on redundant switching states [44]. The modified switching scheme proposed in [45] is used to prevent unwanted high frequency switching which causes high switching loss and failure to the circuit. In the reverse path when the battery is charged by utility power, all the inverter switches are off. In this case the body diodes of the switches make two parallel full-bridge rectifiers.

2.1.2 Bidirectional Full-Bridge Converter

The proposed inverter design requires a larger DC voltage than what the vehicle's battery can provide. As such, an interface is needed to increase the voltage level from the supply allowing 9 [kW] power output at the 120 [V_{rms}] and 6 [kW] power output at the 240 [V_{rms}] to be maintained. This stage needs to provide the 340 [V] required by the inverter stage, referred to as the DC Link bus, using the 240 [V] input from the EV/PHEV's battery with a minimal amount of variance to prevent generation of additional harmonics in the inverter output. An output voltage ripple maximum of 1% was selected for the design. To have ground isolation and voltage boosting a bidirectional full-bridge converter topology, shown in Fig. 2.3, was selected for this design. Proper switching of this bidirectional converter ensures that the converter always operates in continuous conduction mode even when the inductor current is negative. This bidirectional power flow is necessary to allow for the proper exchange of reactive power between the complex load of the inverter and the DC link. Since the converter feeds the inverter stage with complex load whose voltage and current are not necessary in phase, therefore for keeping the dc-link voltage at the desired value we need to provide the discharge path for the dc-link capacitors to compensate the effect of negative reactance power on the dc-link capacitors. This path can be provided with the proper switching of the converter switches. Logical functions given in (2.1) show the gate signal generation for the converter switches. This switching scheme keeps the converter in the continuous conduction mode even when the inductor current is negative.

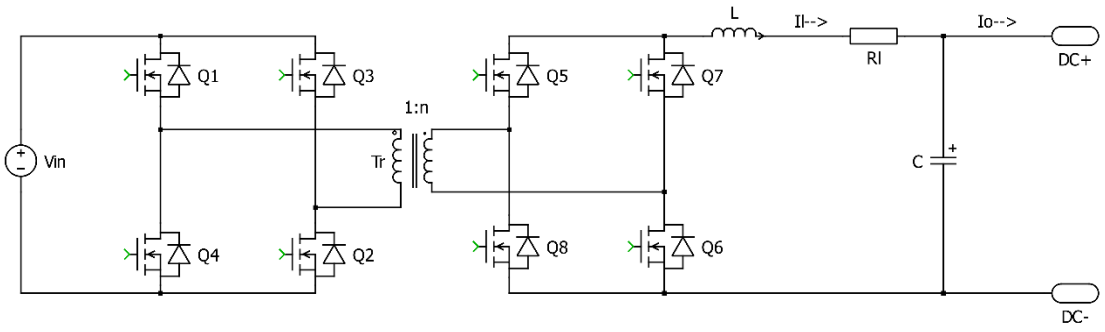

Fig. 2.3 Bidirectional Full-Bridge Converter.

$$
\begin{aligned}
&Q1 = (D > Tri1)\\
&Q4 = \sim Q1\\
&Q3 = (D > Tri2)\\
&Q2 = \sim Q3\\
&\quad Q5{=}Q6{=}HC1\\
&\quad Q7{=}Q8{=}\sim HC1
\end{aligned}
\tag{2.1}
$$

Where *Tri1* and *Tri2* are the two triangular waveforms which act as carrier references for PWM modulation. $HC1$ is a Boolean variable which is True in the first half of the switching cycle and false in the second and D is the duty ratio of the converter.

2.1.3 Dynamic Model of Bidirectional Full-Bridge Converter

Utilizing the state averaging method [46], [47], the dynamic model of the full-bridge converter with switching scheme represented by (2.1) can be written as:

$$L\dot{I}_l = -R_L I_l - V_{out} + 2V_{in}\frac{N_2}{N_1}(D + d_0) \tag{2.2}$$

$$C\dot{V}_{out} = I_l - I_o. \tag{2.3}$$

Where $V_{in}(t) \in \mathbb{R}$ is the average input voltage supplied by the battery, $I_l(t) \in \mathbb{R}$ is the average current through the inductor L and R_L is its series resistance. $V_{out}(t) \in \mathbb{R}$ and $I_o(t) \in \mathbb{R}$ are output voltage and current, respectively. $\frac{N_2}{N_1}$ is the transformer turns ratio. The term d_0 represents an assumed constant disturbance within the switching.

2.2 Backstepping Controller

There are two uncertainties which the bidirectional full-bridge converter system must be capable of adapting for. First, it is assumed that the battery voltage will change as the system discharges. Secondly, it is assumed that the load may also vary as the consumers vary their power consumption. In an effort to meet the input voltage requirements set by the ANPC inverter stage, a novel backstepping control scheme is developed for the bidirectional full-bridge converter stage. This controller works to maintain a fixed DC link voltage in the presence of a varying battery state of charge (SOC) and variable load. Recent works such as [5], [48] have shown that increased performance is achieved if the control scheme also compensates for an unknown disturbance within the PWM scheme, therefore this development includes the additional adaptive term to compensate for this disturbance.

2.2.1 Control Objectives

A control input $D(t) \in \mathbb{R}$ for the bidirectional full-bridge converter, with the dynamic model given in (2.2) and (2.3), is developed such that the output voltage of the

converter,$V_{out}(t) \in \mathbb{R}$, tracks a desired output voltage, $V_d(t) \in \mathbb{R}$, in the presence of an unknown complex load and a constant disturbance in the system.

2.2.2 Assumptions

There are several assumptions that must be made for this controller design:

The bidirectional converter switching scheme is according to (1). Therefore the converter is always in the continuous conduction mode.

- The signals $V_{in}(t)$, $V_{out}(t)$, $I_o(t)$,and $I_l(t)$ are measurable.
- The parameters R_L, L, and C are known constants.
- The desired output voltage trajectory signal, $V_d(t)$, and its first and second derivative are bounded, $V_d,\ \dot{V}_d,\ \ddot{V}_d \in \mathcal{L}_\infty$.
- The output current and its derivative are bounded, $I_o(t), \dot{I}_o(t) \in \mathcal{L}_\infty$.

2.2.3 Controller Design

In order to meet the desired voltage, tracking error signal $e(t) \in \mathbb{R}$ and auxiliary error signal $\eta(t) \in \mathbb{R}$ are defined as:

$$e = V_d - V_{out} \tag{2.4}$$

$$\eta = I_d - I_l \tag{2.5}$$

Where $I_d(t) \in \mathbb{R}$ is an auxiliary control signal which will be designed subsequently. To account for the unknown disturbance, an error signal $\tilde{d}_0 \in \mathbb{R}$ is developed as follows:

$$\tilde{d}_0 = d_0 - \hat{d}_0 \tag{2.6}$$

where $\hat{d}_0 \in \mathbb{R}$ is the estimated disturbance which will be defined subsequently.

Taking the time derivative of (2.4) and (2.5) and substituting for $\dot{V}_{out}$ and $\dot{I}_l$ from (2.2) and (2.3), and multiplying by C and L respectively, the open loop system error can be rewritten as:

$$C\dot{e} = C\dot{V}_d - I_d + \eta + I_o \tag{2.7}$$

$$L\dot{\eta} = L\dot{I}_d + R_l I_l + V_{out} - 2V_{in}\frac{N_2}{N_1}(D + d_o). \tag{2.8}$$

From the subsequent stability analysis, the auxiliary controller, $\mathrm{I_d(t)}$, and the duty ratio of the PWM control signal , $\mathrm{D(t)}$, are defined as in follows:

$$I_d \triangleq C\dot{v}_d + k_1 e + I_o \tag{2.9}$$

$$D \triangleq \frac{1}{V_{in}\frac{N_2}{N_1}}\left[W_1 + e + k_2\eta + k_3 sgn(\eta) - V_{in}\frac{N_2}{N_1}\hat{d}_0\right] \tag{2.10}$$

where

$$W_1 = LC\ddot{V}_d + k_1 L\dot{V}_d + \frac{k_1 L(I_o - I_l)}{C} + R_l I_l + V_{out}. \tag{2.11}$$

where $k_1, k_2, k_3 \in \mathbb{R}^+$ are controller gains. The parameter update law for the unknown disturbance is defined as follows:

$$\dot{\hat{d}}_o \triangleq -k_4\eta V_{in}\frac{N_2}{N_1} \tag{2.12}$$

where $k_4 \in \mathbb{R}^+$ is a positive gain. Substituting (2.7) and (2.8) for $I_d(t)$ and $D(t)$ from (2.9) and (2.10) give us the following closed loop system error equations:

$$C\dot{e} = -k_1 e + \eta \tag{2.13}$$

$$L\dot{\eta} = L\dot{I}_o - e - k_2\eta - k_3 sgn(\eta) - V_{in}\frac{N_2}{N_1}\tilde{d}_o. \tag{2.14}$$

2.2.4 Stability Analysis

Theorem 1: Using the closed loop error system equations found in (2.13) and (2.14), the error signals defined in (2.4) and (2.5) are regulated as follows:

$$e(t), \eta(t) \to 0 \; as \; t \to \infty \tag{2.15}$$

when the following gain condition is met

$$k_3 > L\dot{I}_o. \tag{2.16}$$

Proof: A non-negative scalar function, $S(t) \in \mathbb{R}$ is defined in (2.16).

$$S = \frac{1}{2}Ce^2 + \frac{1}{2}L\eta^2 + \frac{1}{2}k_4^{-1}\tilde{d}_0^2 \tag{2.17}$$

Taking the derivative of (2.17) with respect to time and substituting for the closed loop error signals from (2.13) and (2.14), the expression in (2.18) is obtained for time derivative of $S(t)$ where (2.12) is also utilized.

$$\dot{S} = -k_1 e^2 - k_2\eta^2 - k_3|\eta| + \eta L\dot{I}_o. \tag{2.18}$$

The expression in (2.18) can be upper bounded as follows:

$$\dot{S} \leq -k_1 e^2 - k_2\eta^2 - \left(k_3 - L\dot{I}_o\right)|\eta|. \tag{2.19}$$

Assuming that the control gain k_3 is selected as stated in (2.16), then (2.19) can be further simplified as:

$$\dot{S} \leq -k_1 e^2 - k_2 \eta^2 \tag{2.20}$$

From (2.17) and (2.20) it is clear that $e(t), \eta(t), \tilde{d}_0 \in \mathcal{L}_\infty$ and that $e(t), \eta(t) \in \mathcal{L}_2$. From (2.4) and by considering that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_{out}(t) \in \mathcal{L}_\infty$. Then, from (2.9) and assuming $I_o(t)$, $\dot{V}_d(t) \in \mathcal{L}_\infty$, it is clear that $I_d(t) \in \mathcal{L}_\infty$, hence from (2.5) we can see that $I_l(t) \in \mathcal{L}_\infty$ .From (2.13) and $e(t), \eta(t) \in \mathcal{L}_\infty$ it is clear that $\dot{e}(t) \in \mathcal{L}_\infty$. From (2.6) and because $d_0(t), \tilde{d}_0(t) \in \mathcal{L}_\infty$ it is clear that $\hat{d}_0(t) \in \mathcal{L}_\infty$. From (2.11), it can be shown that $W_1(t) \in \mathcal{L}_\infty$ because $\ddot{v}_d(t), \dot{v}_d(t), I_l(t), V_{out}(t) \in \mathcal{L}_\infty$. Additionally, from (2.10) it is clear that $D(t) \in \mathcal{L}_\infty$. Therefore we have proved that all signals in the closed loop are bounded. Now we will prove that the error signals, $e(t)$ and $\eta(t)$, converge to zero as $t \to \infty$. From (2.13) and $e(t), \eta(t), \in \mathcal{L}_\infty$ it is clear$\dot{e}(t) \in \mathcal{L}_\infty$. From (2.14), and assuming $\dot{I}_o(t) \in \mathcal{L}_\infty$ it is clear that $\dot{\eta}(t) \in \mathcal{L}_\infty$. Since $e(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t), \dot{\eta}(t) \in \mathcal{L}_\infty$, according to the Barbalat's Lemma [49] it is clear that $e(t), \eta(t) \to 0$ as $t \to \infty$.

2.3 Simulation Results

To validate the system design and evaluate the performance of the developed controller numerical simulation using PLECS software is completed. The simulation parameters are presented in Table 2.

Table 2.1 V2G System Parameters

Parameter	Value	Unit	Parameter	Value	Unit
V_{in}	$240 - .05\text{ramp(t)}$	V	C3=C4	200	μF
V_d	340	V	K1	4	-
F_{sw_Conv} (Converter Switching frequency)	50	KHz	K2	2	
F_{sw_Inv} (Inverter Switching frequency)	20	KHz	K3	.01	-
L	100	μH	K4	1	
C	1	mF	Z_1 (Load1 impedance)	$3.9 + j1.88$	Ω
C1=C2	2	mF	Z_2 (Load2 impedance)	$13 + j6.4$	Ω

To facilitate the simulation, the converter was operated with a fixed duty cycle for $t < 0.04\ [sec]$. After this the duty cycle generated by the controller was applied to the converter. At $t = 0.08\ [\text{sec.}]$ the simulated load changes from $Z_1 = 3.9 + j1.88\ [\Omega]$ to $Z_2 = 13 + j6.4\ [\Omega]$. To simulate changes in the battery SOC, the input voltage to the converter stage V_{in} reduces linearly with a slope of 0.05[V/S] from its initial value, 240[V]. Fig. 2.4 shows the tracking performance of the converter. Signals $e(t)$ and duty cycle, D(t), are seen in Fig. 2.5 and 2.6 respectively. From these figures it is clear that the converter and its developed controller work well within the desired parameters in closed loop control, achieving an output voltage 340 [V] with a very low ripples. Comparing the inductor current with its desired value I_d in Fig. 2.7, it can be seen that the converter is always in the continuous conduction mode and that control is maintained even when the inductor current is negative. Fig. 2.8 shows that the estimated disturbance in duty ratio converges to a constant value.

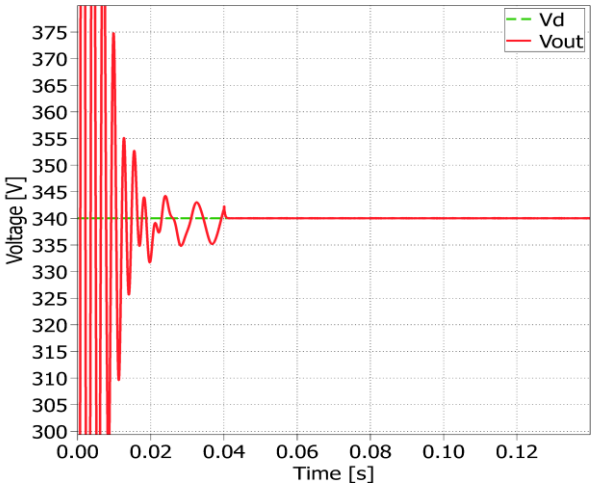

Fig. 2.4 Output voltage,$V_{out}(t)$, and the desired voltage, $V_d(t)$, of Bidirectional Full-Bridge Converter.

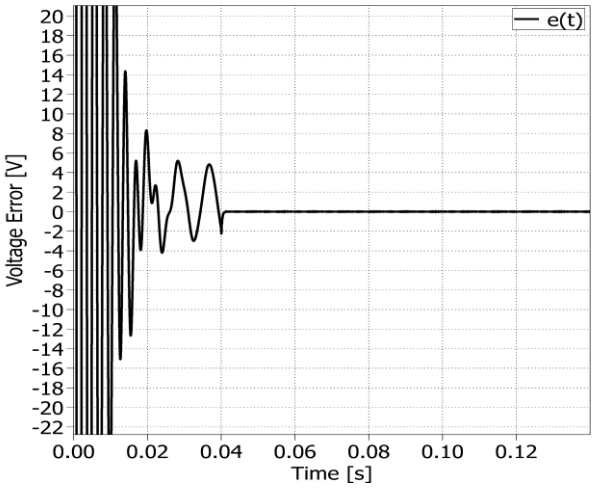

Fig. 2.5 Voltage tracking error, $e(t)$ of Bidirectional Full-Bridge Converter.

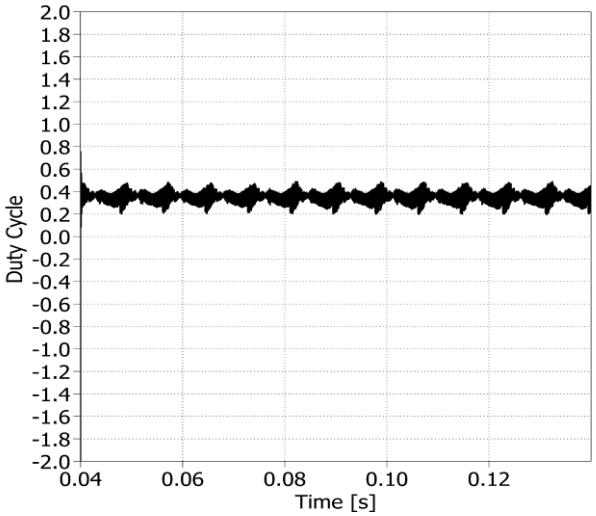

Fig. 2.6 Control duty cycle, $D(t)$, of Bi-Directional Full-Bridge Converter.

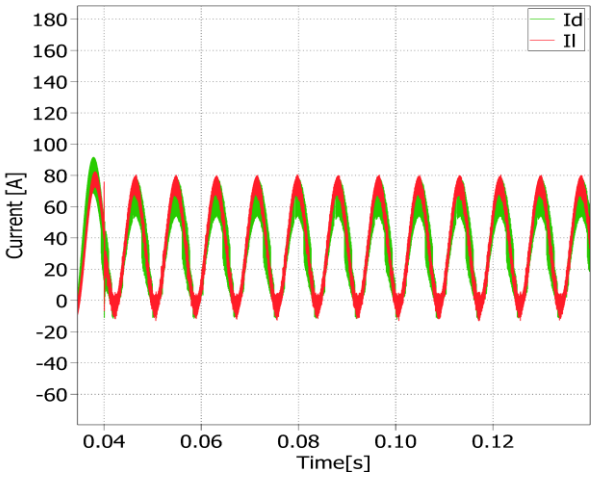

Fig. 2.7 Bidirectional Full-Bridge Converter Inductor Current.

The level-shifted four-carrier PWM scheme with unity modulation index and 20 kHz carrier frequency (f_{tri}) is selected for system level simulation of the ANPC inverter. The line-to-neutral and line-to-line output voltage of the inverter are shown in Fig. 2.9 and 2.10 respectively. The normalized Fourier coefficients of the line-to-line output voltage are illustrated in Fig. 2.11. As can be seen in Fig. 2.11, the individual voltage distortion for $f < 2f_{tri} = 40$ kHz is less than 0.03% which is well within the harmonic limits set by IEEE

519. Implementation of a simple LC filter at the output fulfills total voltage distortion limits of IEEE 519 and also removes high frequency harmonics around $f = 2f_{tri}$.

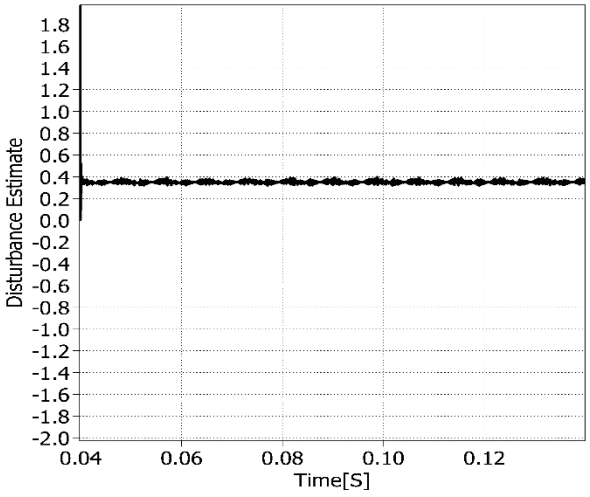

Fig. 2.8 Bidirectional Full-Bridge Converter Estimated Disturbance.

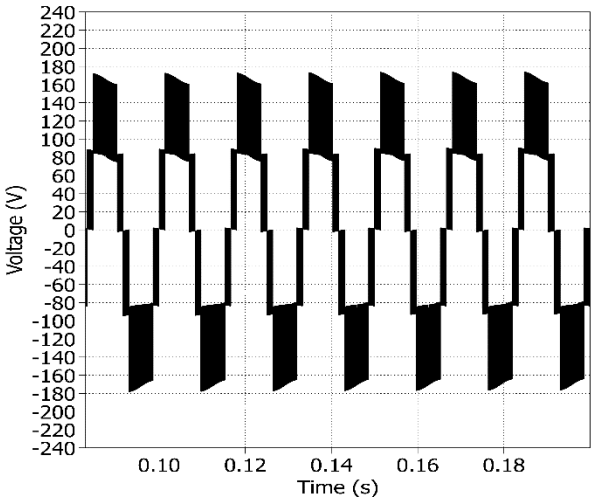

Fig. 2.9 ANPC Inverter Line to Neutral Output Voltaege.

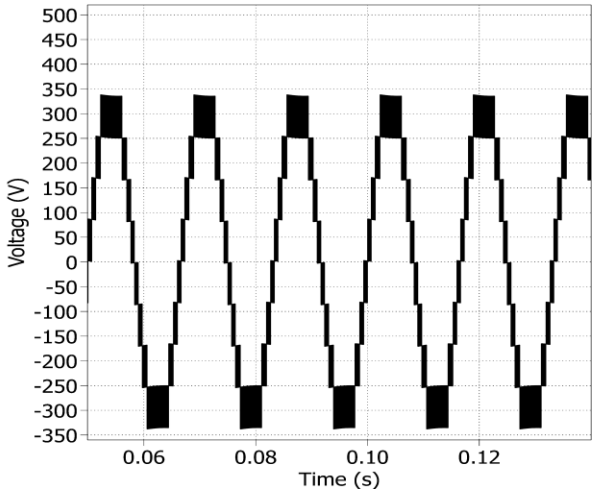

Fig. 2.10 ANPC Inverter Line to Line Output Voltaege .

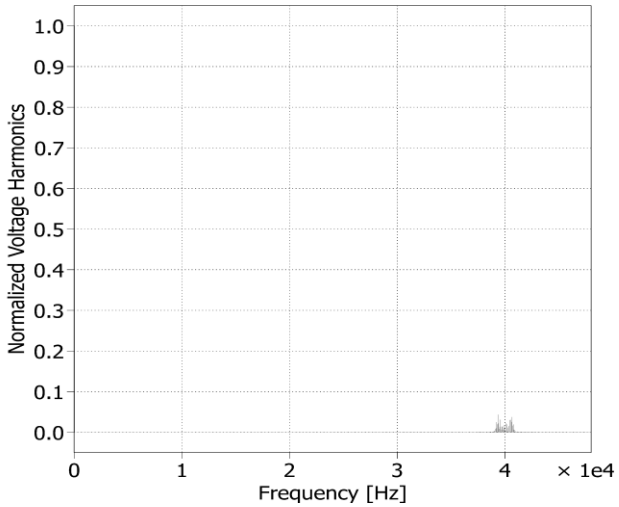

Fig. 2.11 Output Voltage Normalized Harmonics with Respect to Fundamental.

2.4 Summary

A typical DC:AC conversion system consists of two stages, a DC:DC converter to generate the necessary bus voltage followed by an inverter which generates the desired AC output. A modification of this system is proposed for the purpose of reducing switching losses. The proposed two-stage system consists of a buck converter which produces a

mixed (DC+AC) signal which is fed to a traditional inverter. This mixed signal is designed such that it reduces the switching loss across the inverter switches while still providing the necessary voltage for the inverter input. Backstepping controllers are designed to achieve output voltage tracking objectives for both stages. Lyapunov stability analysis and simulation results validate these controller designs. Efficiency and THD comparisons are made between the typical and modified systems. The results show that all the system components of this design work as expected from analytical results. The individual voltage distortion was kept low and due to its location at higher harmonics can be easily filtered out to fulfill total voltage distortion limits of IEEE 519. The novel backstepping controller is capable of controlling the DC to DC converter stage in presence of varying battery SOC, uncertain complex load and switching disturbance. The split phase output voltage has the desired frequency and magnitudes to replace household backup generator, validating the system's use for V2H applications. The reverse path provides battery charging circuit to store energy in the vehicle battery. The system's design is straightforward, relying on isolated power electronic designs and is appropriately controllable.

CHAPTER 3

ENERGY EFFICIENT DC TO AC POWER CONVERSION

A typical DC:AC conversion system consists of a DC:DC converter to step-up/down the DC voltage level that is then fed to a voltage source inverter (VSI). The purpose of the converter is to provide a fixed DC bus voltage to the subsequent stage. The VSI then converts the regulated and fixed DC voltage to the appropriate AC voltage output.

An alternate approach is proposed in which the converter stage provides a mixed (DC+AC) signal to the VSI stage. This mixed signal is designed such that it reduces the switching loss across the VSI switches while still providing the necessary voltage for the inverter input. A bidirectional Buck converter was chosen to provide this mixed signal from the DC input voltage for the proposed design.

Many solutions have been developed to reduce switching losses in converter and inverter switches, most commonly by the use of snubbers or resonant techniques [50]. The aim of these methods are to ensure that the voltage and/or current across the switch are zero at the time of switching. This is usually achieved by adding additional inductors and/or capacitors to a classical H-bridge hard-switching solution as well as more complicated switching schemes seen in [51], [52]. In this study two different methods are utilized simultaneously to reduce the power loss in the converter and inverter stages, respectively. In general, it is required that the desired output voltage of a VSI be less than or equal to its

input voltage. An exception to this requirement is over-modulation whereby it is possible for a VSI to exceed this limit at the cost of a significant increase in THD. Because this works against the end objective over-modulation is not considered in this work. For a VSI using a fixed DC input voltage, this requirement means that the bus voltage must be greater than or equal to the maximum output voltage magnitude. This bus voltage determines the switch blocking voltage and therefore to a large degree the switching losses [53]. By replacing this fixed DC input with a time-varying voltage that still meets the voltage requirement mentioned, but is less than or equal to the DC voltage at all points in the cycle, losses can be greatly reduced.

The proposed method for reducing switching loss in the converter stage is to utilize a lower switching frequency. In the VSI stage it is necessary to operate at a high switching frequency to both fulfill THD requirements and improve system dynamics, however this is not the case for the converter stage. So long as the output voltage of the converter meets the voltage requirement mentioned above, any non-idealities in the output voltage of the converter can be compensated for by the controller of the inverter.

In the past decade, much attention has been paid to the closed-loop regulation of switch-mode converters and inverters to achieve good dynamic response under different types of loads. Methods such as linear control [54] , passivity-based control [55], Lyapunov-based control [56], optimal multi-loop linear resonant control [47], sliding-mode control [46], [53], [21] etc. have all been utilized for this problem. In this chapter two backstepping controllers are utilized for voltage tracking of the converter and inverter stages [57]. The buck converter controller ensures that the output voltage tracking objective is met given knowledge of input voltage and circuit parameters as well as

measurements for output voltage, output current, and inductor current. The controller also incorporates an adaptive estimator which compensates for a fixed, unknown disturbance in the system. The VSI controller also ensures output voltage tracking and disturbance estimation. This controller depends on knowledge of the circuit parameters, as well as measurements for input voltage, output voltage, inductor current, and output current.

3.1 System Design

A series of power electronic interfaces (PEI) are chosen to provide the 120 [V_{rms}], 60 [Hz] single phase AC voltage from the DC supply as seen in Fig. 3.1. A bidirectional buck converter steps down the DC supply as determined by its controller to generate the desired mixed signal voltage to be fed to the VSI. In the next stage, the VSI generates the required AC voltage from the mixed input voltage with an acceptable THD to meet IEEE 519 harmonic distortions limitations.

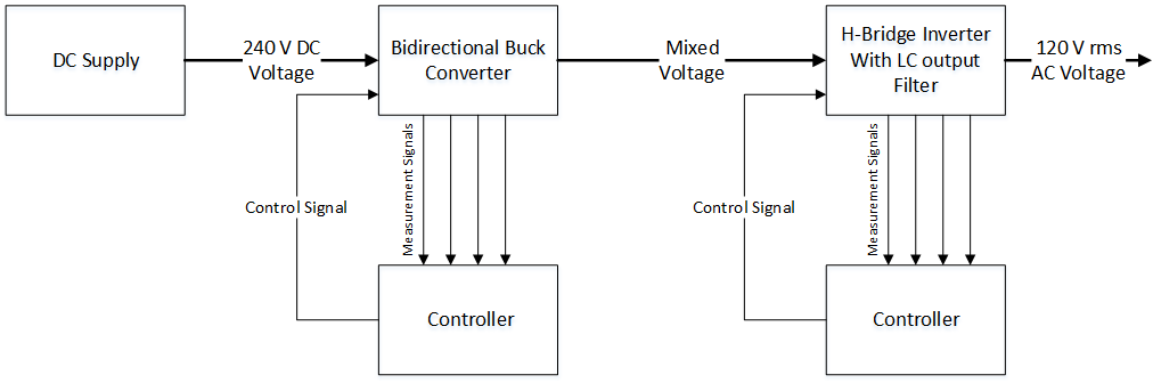

Fig. 3.1 System block diagram for generating 120 [V_{rms}] AC voltage from 240V DC input.

3.1.1 Bidirectional Buck Converter

The Buck Converter is a commonly used switched mode power supply designed for step-down voltage operation. These power supplies often use control systems to improve performance and stability. For this work, an adaptive control design is utilized. Adaptive control allows the system to compensate for an unknown disturbance.

The subsequent controller design is based upon a circuit model which assumes operation in the continuous conduction mode (CCM). However, due to the nature of the mixed signal voltage trajectory it is probable that inductor current may reach zero which would otherwise force the circuit into discontinuous conduction mode (DCM), thereby invalidating the assumed system model. For this purpose a bidirectional buck converter topology is proposed to keep the converter in CCM allowing inductor current to become negative. The circuit diagram for this bidirectional buck converter is shown in Fig. 3.2. Although switching commands to IGBT D1 and IGBT D2 are logical complements, in practical implementation we should consider a dead time between these two signals to prevent shoot-through conditions.

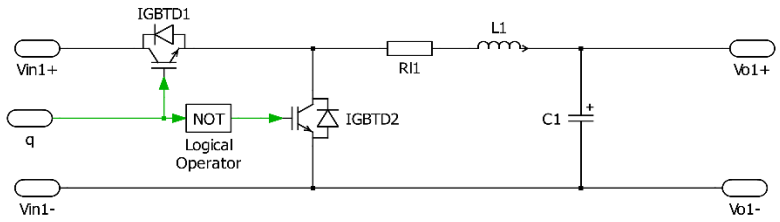

Fig 3.2 Bidirectional Buck converter.

Though a linear controller such as a type3 controller [58] is capable of achieving voltage tracking for a buck converter it was determined that such a controller is not stable with a bidirectional buck converter, especially given a mixed signal trajectory. Therefore

a nonlinear backstepping controller is proposed for this design. Typically the control of bidirectional buck converters focus only on unidirectional power flow and the control is separated into two modes of operation, sinking and sourcing. However, in this application within one cycle of the system operation we may have energy flow in both directions. In this work a single backstepping controller will be designed which is capable of controlling the converter under both modes of operation.

The dynamic model of a bidirectional buck converter system as seen in Fig. 3.2 is described by the following instantaneous circuit equations:

$$C_1 \dot{v}_{o1} = i_{l1} - i_{o1} \tag{3.1}$$

$$L_1 \frac{di_{l1}}{dt} = -R_{l1} i_{l1} - v_{o1} + v_{in1} q \tag{3.2}$$

where $L_1 \in \mathbb{R}$ is the inductance, $C_1 \in \mathbb{R}$ is the capacitance, $v_{in1}(t) \in \mathbb{R}$ is the input supply voltage, $i_{l1}(t) \in \mathbb{R}$ is the inductor current, $v_{o1}(t) \in \mathbb{R}$, is the output voltage, $q(t) \in (0,1)$ is the switched control signal, and $i_{o1}(t) \in \mathbb{R}$ is the output current that feeds H-Bridge inverter. This model is valid for both positive and negative values of inductor current. State averaging methods [47], [46] can be utilized to convert the instantaneous model defined in (3.1), (3.2), to an average dynamic model of the system when a pulse width modulation (PWM) scheme is utilized for $q(t)$ [58]. The average model over a PWM switching period can be written as follows:

$$C_1 \dot{V}_{o1} = I_{l1} - I_{o1} \tag{3.3}$$

$$L_1 \dot{I}_l = -R_{l1} I_{l1} - V_{o1} + V_{in1} D_1 \tag{3.4}$$

where $V_{in1}(t) \in \mathbb{R}$ is the average supply voltage, $I_{l1}(t) \in \mathbb{R}$ is the average inductor current, $I_{o1}(t) \in \mathbb{R}$ is the average output current, $V_{o1}(t) \in \mathbb{R}$ is the average output voltage, and $D_1(t) \in \mathbb{R}$ is the duty ratio of the control signal $q(t)$. A semi-constant unknown disturbance, d_{01} , is considered as PWM disturbance that needs to be accounted for by the control scheme. With this, we write (3.4) as follows:

$$L_1\dot{I}_{l1} = -R_{l1}I_{l1} - V_{o1} + V_{in1}(D_1 + d_{01}). \tag{3.5}$$

3.1.2 Trajectory Signal Design for Bidirectional Buck converter

In this section a desired voltage trajectory $V_{d1}(t)$ of the output voltage $V_{o1}(t)$of the bidirectional buck converter will be designed such that it minimizes the switching losses in the VSI stage. The inverter generates an AC voltage from the input voltage. As discussed previously, the inverter is capable of generating any instantaneous output voltage so long as the input voltage to the inverter is higher than the absolute value of the desired output. This fact motivates us to provide a varying input to the inverter instead of a fixed DC voltage to reduce the switching loss in the high switching frequency stage of the system. Fig. 3.3 shows the required AC voltage of the inverter and a possible input voltage to the inverter of the form $|200\sin(2\pi 60t)|$. The maximum value of this input is chosen such that the output voltage is generated with an effective amplitude modulation index of $\frac{120\sqrt{2}}{200} = .85$ in the inverter stage and maximum duty ratio of $\frac{200}{240} = .83$ in the converter stage.

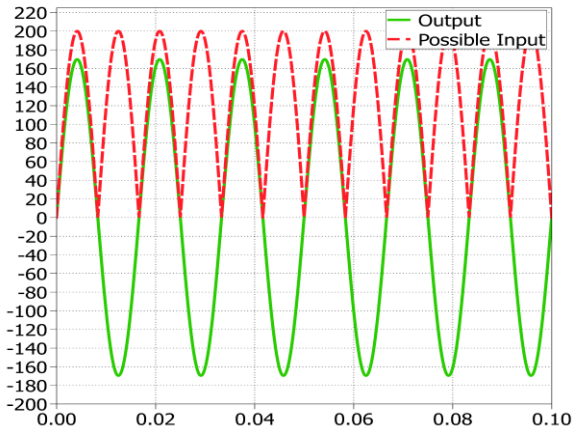

Fig. 3.3 Possible inverter input and output signals.

The subsequent control development will require $V_{d1}(t), \dot{V}_{d1}(t), \ddot{V}_{d1}(t) \in \mathcal{L}_\infty$. For this design a trajectory signal composed of the first two harmonics of the desired input plus a constant was chosen. This constant value gives the inverter controller more flexibility in its output amplitude. The resulting voltage trajectory for the buck converter is as follows

$$V_{d1}(t) = 125.81 + 20 + 83.89\sin(2\pi 120t) = 145.81 + 83.89\sin(2\pi 120t).$$

Where 125.81 and $83.89\sin(2\pi 120t)$are the first and second harmonics of the desired signal and 20 is the constant value added to the trajectory signal. More harmonics can be added to the trajectory signal but the performance improvement in terms of switching loss reduction in the inverter is insignificant. Fig. 3.4 shows the designed V_{d1} along with the absolute value of the output voltage of the inverter.

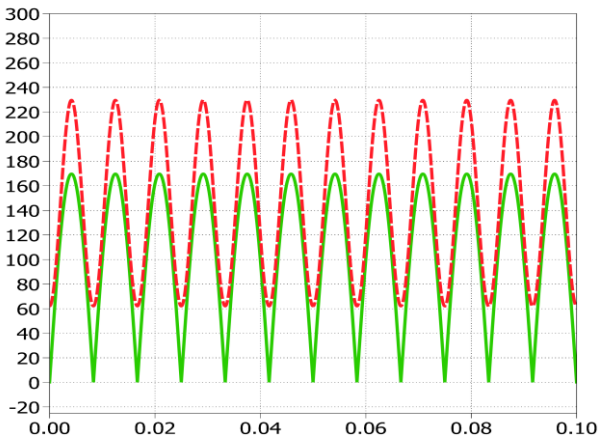

Fig. 3.4 Trajectory signal and absolute value of output AC signal.

3.1.3 H-Bridge Inverter

A VSI as seen in Fig. 3.5, is used to convert the mixed voltage output of the buck converter into an AC output voltage with the addition of a simple LC filter. A unipolar PWM switching scheme was selected for this design. The proposed topology is capable of the bidirectional energy flow necessary to effectively drive a complex load. In order to design the controller for an H-Bridge inverter an analytical control model must be created.

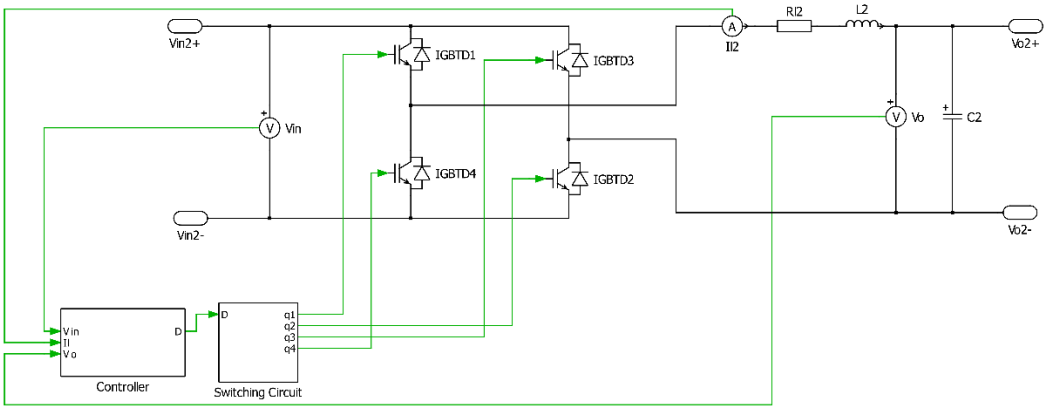

Fig. 3.5 H-Bridge inverter.

Following the assumption that a unipolar switching scheme for PWM is utilized, q4 and q3 are logical complement to q1 and q2 respectively and the inverter operates in 3 different states where q1, q2, q3 and q4 are logical IGBT gate signals.

State1: For q1=1 and q2=1 the input voltage to the LC filter is V_{in}.

State2: For q1= q2=0 the input to the LC filter is $-V_{in2}$

State3: For q1=1, q2=0 or q1=0, q2=1 the input voltage to the output filter is 0.

Applying the state averaging method, and considering a constant PWM disturbance, d_{02}, the average model for an H-Bridge inverter can be written as follows:

$$C_2\dot{V}_{o2} = I_{l2} - I_{o2} \tag{3.6}$$

$$L_2\dot{I}_{l2} = -R_{l2}I_{l2} - V_{o2} + V_{in2}(D_2 + d_{02}). \tag{3.7}$$

Where $V_{in2}(t) \in \mathbb{R}$ is the average supply voltage, $I_{l2}(t) \in \mathbb{R}$ is the average inductor current, $V_{o2}(t) \in \mathbb{R}$ is the average output voltage, and $D_2(t) \in (-1,1)$ is the duty ratio. A positive duty ratio means the inverter switches between state 1 and 3 and a negative duty cycle means the inverter switches between state 2 and 3.

We want to develop a control input, $D_2(t)$ that enables the inverter stage output voltage, $V_{o2}(t)$, to track a desired output voltage, $V_{d2}(t)$,in the presence of an unknown load and a constant disturbance in the system. In this application $v_{d2}(t)$ is a sinusoidal waveform with 60Hz frequency and $120\sqrt{2}$ amplitude.

3.2 Control Design

Comparing equations (3.3-3.5) which models dynamics of bidirectional buck converter with equations (3.6-3.7) which models dynamics of H-Bridge converter, we can see both systems are modeled with the same equations except that the range of duty ratio is (0,1) for buck converter and (-1,1) for H-Bridge inverter. Therefore we can design the same controller for both converters. Henceforth the subscript $x \in \{1,2\}$is used to denote whether the parameters belong to the converter ($x = 1$) or the inverter ($x = 2$). To generalized the controller development we consider a constant duty ratio disturbance, d_{ox}, in our equations. To facilitate the control development, the following assumptions are made.

Assumption 1: $I_{lx}(t), I_{ox}(t), V_{ox}(t), V_{inx}(t)$ are measurable.

Assumption 2: $C_x,\ L_x, R_{lx}$ are known system parameters.

Assumption 3: $V_{dx}(t), \dot{V}_{dx}(t), \ddot{V}_{dx}(t) \in \mathcal{L}_\infty$, where $V_{dx}(t)$ is the desired output voltage trajectory.

Assumption 4: The duty cycle disturbance is slowly time varying in the sense that $\dot{d}_{0x}(t) \approx 0$.

Assumption 5: The output current is continuous, $\dot{I}_{0x}(t) \in \mathcal{L}_\infty$.

Our control objective is to design $D_x(t)$ such that $V_{ox}(t) \to V_{dx}(t)$ as $t \to \infty$.

3.2.1 Error System Development

To meet the defined control objective, tracking errors signals $\mathrm{e}_x(\mathrm{t}),\ \eta_x(\mathrm{t}) \in \mathbb{R}$ are defined as follows:

$$e_x \triangleq V_{dx} - V_{ox} \tag{3.8}$$

$$\eta_x \triangleq I_{dx} - I_{lx} \tag{3.9}$$

where $I_{dx}(t) \in \mathbb{R}$ is a subsequently designed auxiliary control signal. Taking the time derivative of equation (3.8) and (3.9), and utilizing the average system dynamics from (3.6) and (3.7), the open loop error systems can be written as follows:

$$C_x \dot{e}_x = C_x \dot{V}_{dx} - I_{dx} + \eta_x + I_{ox} \tag{3.10}$$

$$L_x \dot{\eta}_x = L_x \dot{I}_{dx} + R_{lx} I_{lx} + V_{ox} - V_{inx}(D_x + d_{0x}). \tag{3.11}$$

Since the duty ratio disturbance d_{0x} is unknown, we define the disturbance error $\tilde{d}_{0x}(t) \in \mathbb{R}$ as follows:

$$\tilde{d}_{0x} \triangleq d_{0x} - \hat{d}_{0x} \tag{3.12}$$

where $\hat{d}_{0x}(t) \in \mathbb{R}$ is the disturbance estimate.

3.2.2 Control Input Design

The control inputs found in (3.10) and (3.11) are developed based on the subsequent stability analysis. The auxiliary control input $I_{dx}(t)$ found in (3.10) is designed as follows:

$$I_{dx} \triangleq C_x \dot{V}_{dx} + k_{1x} e_x + I_{ox} \tag{3.13}$$

where $k_{1x} \in \mathbb{R}^+$ is a control gain. The control law defined in (3.13) is substituted into (3.10) and the following closed loop error system for $e_x(t)$ can be written

$$C_x \dot{e}_x = -k_{1x} e_x + \eta_x \tag{3.14}$$

As seen in (3.11), the time derivative of I_{dx} is required. Taking derivative of (3.13) and substituting in (3.11) we have:

$$L_x\dot{\eta}_x = W_{1x}(\cdot) + L_x\dot{I}_{ox} - V_{inx}D_x - V_{inx}\tilde{d}_{0x} - V_{inx}\hat{d}_{0x} \tag{3.15}$$

where

$$W_{1x} = L_xC_x\ddot{V}_{dx} + k_{1x}L_x\dot{V}_{dx} - \frac{k_{1x}L_xI_{lx}}{C_x} + \frac{k_{1x}L_xI_{ox}}{C_x} + R_{lx}I_{lx} + V_{ox}. \tag{3.16}$$

The duty ratio of the PWM control signal for the power converter $D_x(t)$ is defined as follows:

$$D_x \triangleq \frac{1}{V_{inx}}\left[W_{1x} + e_x + k_{2x}\eta_x + k_{3x}sgn(\eta_x) - V_{inx}\hat{d}_{0x}\right] \tag{3.17}$$

where $k_{2x}, k_{3x} \in \mathbb{R}^+$ are the control gains.

The parameter update law for the unknown disturbance is defined as follows

$$\dot{\hat{d}}_{0x} \triangleq -k_{4x}\eta_xV_{inx} \tag{3.18}$$

Substituting (3.17) into (3.15) provides the following closed loop error system for $\eta(t)$

$$L_x\dot{\eta}_x = L_x\dot{I}_{0x} - e_x - k_{2x}\eta_x - k_{3x}sgn(\eta_x) - V_{inx}. \tag{3.19}$$

3.2.3 Stability Analysis

Theorem 1: Using the closed loop error system equations found in (3.14) and (3.19), the error signals defined in (3.8) and (3.9) are regulated as follows

$$e_x(t), \eta_x(t) \to 0 \; as \; t \to \infty.$$

Proof: A non-negative scalar function, $S_x(t) \in \mathbb{R}$ is shown in (3.20).

$$S_x = \frac{1}{2}c_x e_x^2 + \frac{1}{2}L_x\eta_x^2 + \frac{1}{2}k_{4x}^{-1}\tilde{d}_{0x}^2 \tag{3.20}$$

Taking the derivative of (3.20) with respect to time and substituting the closed loop error signals from (3.14) and (3.19), the expression in (3.21) is obtained where (3.18) is also utilized.

$$\dot{S}_x = -k_{1x}e_x^2 - k_{2x}\eta_x^2 - k_3|\eta_x| + \eta_x L_x \dot{I}_{ox}. \tag{3.21}$$

The expression in (3.21) can be upper bounded as follows:

$$\dot{S}_x \leq -k_{1x}e_x^2 - k_{2x}\eta_x^2 - \left(k_{3x} - L_x\dot{I}_{ox}\right)|\eta_x|. \tag{3.22}$$

Assuming that the control gain k_3 is selected as stated in (3.23), then (3.22) can be further simplified as (3.24).

$$k_{3x} > L_x\dot{I}_{ox} \tag{3.23}$$

$$\dot{S}_x \leq -k_{1x}e_x^2 - k_{2x}\eta_x^2 \tag{3.24}$$

From (3.20) and (3.24) it is clear that $e_x(t), \eta_x(t), \tilde{d}_{0x} \in \mathcal{L}_\infty$ $\mathcal{L}_\infty$ and that $e_x(t), \eta_x(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$. From (3.8) and by definition that $V_{dx}(t) \in \mathcal{L}_\infty$, therefore $V_{ox}(t) \in \mathcal{L}_\infty$. Then, from (3.13) assuming $I_{ox}(t)$, $\dot{V}_{dx}(t) \in \mathcal{L}_\infty$, it is clear that $I_{dx}(t) \in \mathcal{L}_\infty$, hence from (3.9) we can see that $I_{lx}(t) \in \mathcal{L}_\infty$ .From (3.14) and $e_x(t), \eta_x(t) \in \mathcal{L}_\infty$ it is clear that $\dot{e}_x(t) \in \mathcal{L}_\infty$. From (3.12) and because $d_{0x}(t), \tilde{d}_{0x}(t) \in \mathcal{L}_\infty$ it is clear that $\hat{d}_{0x}(t) \in \mathcal{L}_\infty$. From (3.16), it can be shown that $W_{1x}(t) \in \mathcal{L}_\infty$ because $\ddot{v}_{dx}(t), \dot{v}_{dx}(t), I_{lx}(t), V_{ox}(t) \in \mathcal{L}_\infty$. Additionally, from (3.17) it is clear that $D_x(t) \in \mathcal{L}_\infty$. From these bounding statements it is clear that all signals in the closed loop are bounded. From (3.14) and $e_x(t), \eta_x(t), \in \mathcal{L}_\infty$ it

is clear $\dot{e}_x(t) \in \mathcal{L}_\infty$. From (3.16), and assuming $\dot{I}_{ox}(t) \in \mathcal{L}_\infty$ it is clear that $\dot{\eta}_x(t) \in \mathcal{L}_\infty$. Since $e_x(t), \eta_x(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}_x(t), \dot{\eta}_x(t) \in \mathcal{L}_\infty$, Barbalat's Lemma [49] is utilized to prove that $e_x(t), \eta_x(t) \to 0 \ \ as\ t \to \infty$.

3.3 Simulation Results

To validate the system design, and control development a numerical simulation is performed. The PLECS toolbox is used with Matlab/Simulink to model the instantaneous circuit dynamics of each interface including the control schemes.

3.3.1 Bidirectional Buck converter

The parameters for the converter and its control scheme are summarized in Table 3.1.

Table 3.1 Bidirectional Buck Converter Simulation Parameters

Parameter	Value	Units
L_1	500	µH
C_1	470	µF
F_{sw1}	5	kHz
V_{in1}	240	V
k_{11}	0.05	-
k_{21}	0.5	-
k_{31}	1	-
k_{41}	0.1	-

Tracking performance is seen in Fig. 3.6. Signals $e_1(t)$ and duty cycle, D_1 (t), are seen in Fig. 3.7 and 3.8 respectively. From these figures it is clear that the control objective is met. From Fig. 3.9 it is clear that the inductor passes the current in both source to the sink direction and vice versa within one cycle of operation.

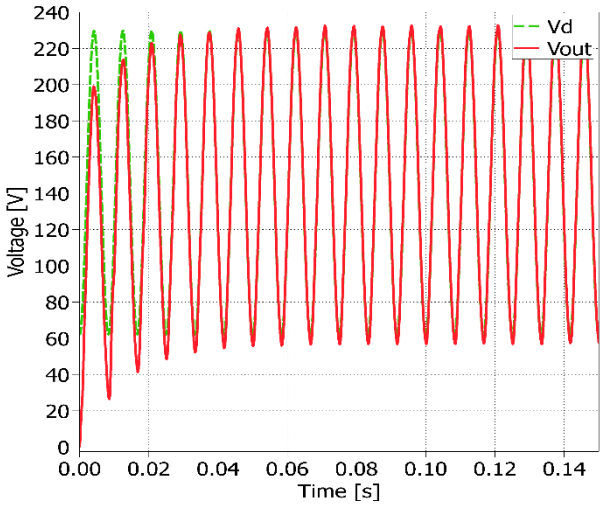

Fig. 3. 6 Converter output voltage and the desired voltage.

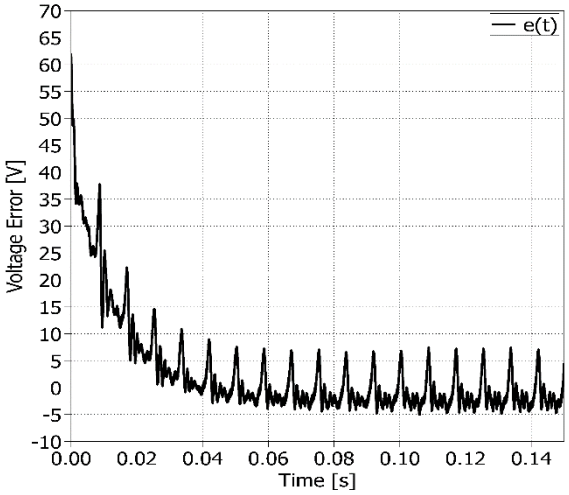

Fig. 3.7 Converter voltage tracking error.

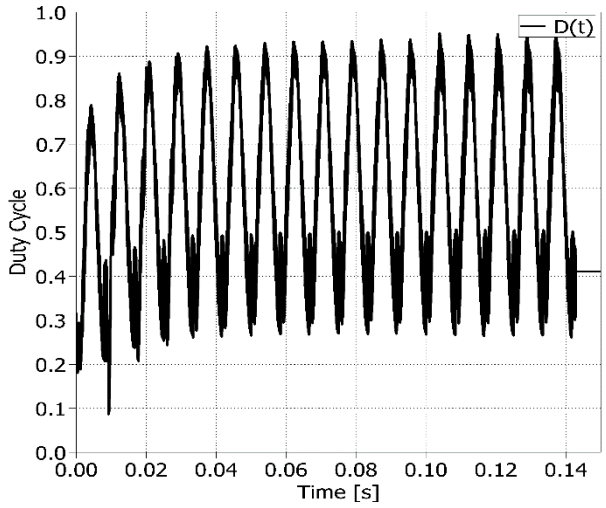

Fig. 3.8 Converter control duty cycle.

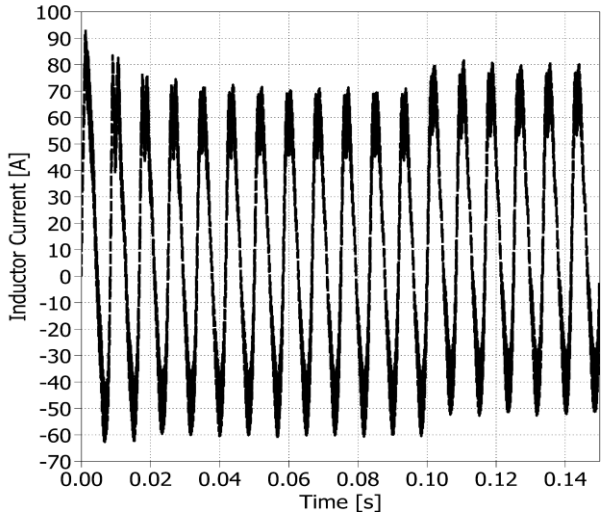

Fig. 3.9 Converter inductor current.

3.3.2 H-Bridge Inverter

The inverter's operation begins at t=0 [s] with $Z_{Load} = 10 + j4.8\,[\Omega]$ load impedance. In section IV we assumed that the output current is continuous, $\dot{I}_{o2}(t) \in \mathcal{L}_\infty$.This particularly means that the load impedance is constant and time-invariant. When this is not the case, the controllers still perform acceptably. In order to simulate the changes

in the load impedance, a parallel 16Ω resistor is switched into the circuit at t=0.1[s]. The effect of this change in the load impedance is illustrated in both inverter and converter stage results.

Table 3.2 H-Bridge Inverter Simulation Parameters

Parameter	Value	Units
L_2	104	µH
C_2	690	µF
F_{sw2}	100	kHz
V_{in2}	1	-
k_{12}	0.1	-
k_{22}	0.1	-
k_{32}	10	
k_{42}	0.1	-

Fig. 3.11, 3.12, 3.13 and 3.14 illustrate the tracking performance, signals $e_2(t)$, $D_2(t)$ and $i_{l2}(t)$ of the inverter respectively. These figures show that, despite the changing load impedance the controller behavior is satisfactory. The simulation waveforms show that the designed circuit operates well within the desired parameters in closed loop control.

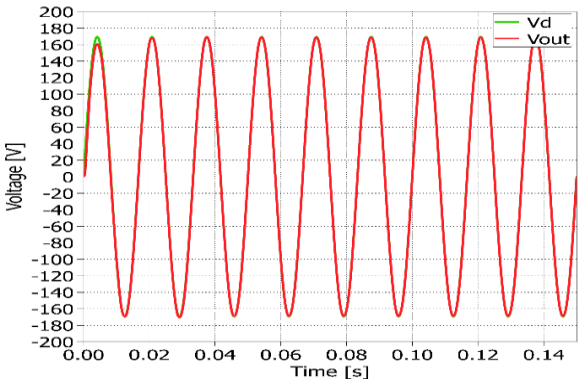

Fig. 3.10 Inverter output voltage and the desired voltage .

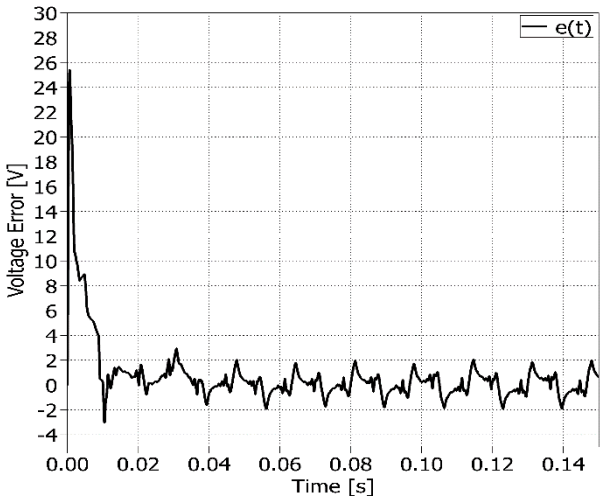

Fig. 3.11 Inverter voltage tracking error.

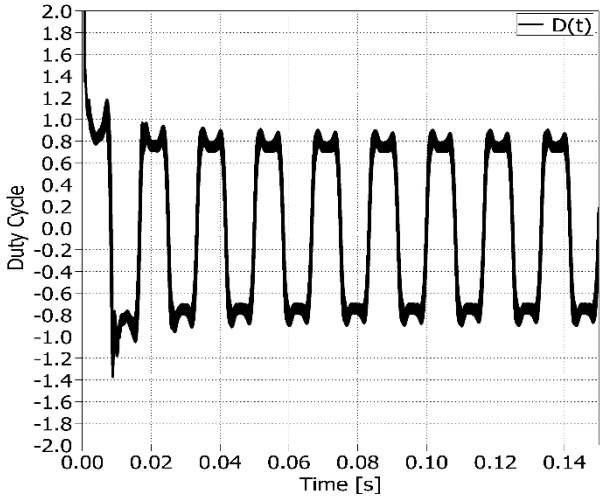

Fig. 3.12 Inverter control duty cycle.

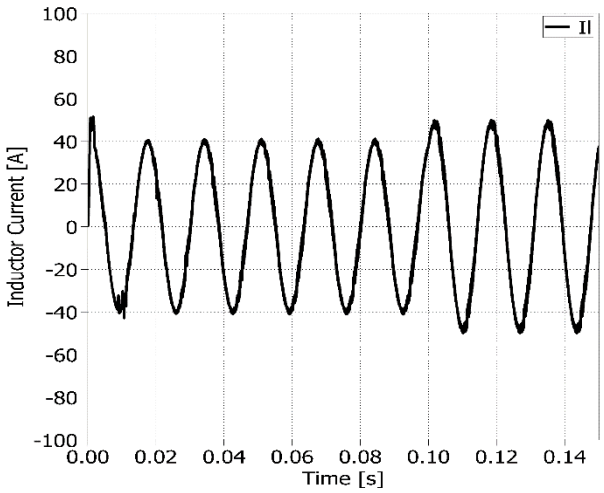

Fig. 3.13 Inverter inductor current.

3.3.3 Switching Loss

To evaluate the performance of the system in terms of switching loss reduction the thermal model and parameters of a commercially available IGBT, *Infineon IKW25N120T2*, is used in the simulation. Table 3.3 compare the switching loss of the system described in section II, referred to as the two-stage PEI, with a system that only utilizes an H-Bridge inverter to generate an AC output voltage from a fixed 240 V input DC voltage, referred to as the one-stage PEI. As it can be seen in table 3.3 the switching loss of the proposed two-stage PEI is almost half of that of the one-stage PEI. As it can be seen in The envelop in the two-stage PEI has a softer shape and semi-sinusoidal form than that of the one-stage PEI . This effect results in a distortion at the output voltage of the two-stage PEI.

3.3.4 Harmonic Distortions

Table 3.4 gives the individual voltage distortion for first five harmonics for both the one-stage and two-stage PEI systems. As it can be seen the individual voltage distortion

is less than 0.1% which meets the harmonic limits of the IEEE 519 ($< 3\%$) . The total harmonics distortion of output voltage is 0.3 % and 0.149 % for the one-stage and two-stage PEI systems respectively which fulfills total voltage distortion limits of IEEE 519 (THD<5%).

Table 3.3 Switching Power Loss Comparison

PEI	Switching Power Loss	
	One-Stage PEI	Two-Stage PEI
Bidirectional Buck	-	20W
H-Bridge	400W	150W
Total	400W	170W

Table 3.4 Harmonic Distortions Comparison

n	$f_n(Hz)$	Distortion	
		One-Stage PEI	Two-Stage PEI
2	120	0.006 %	0.025 %
3	180	0.15 %	0.025 %
4	240	0.009 %	0.008 %
5	300	0.2 %	0.053 %
6	360	0.002 %	0.019 %
THD		0.3 %	0.149 %

3.4 Summary

A two-stage PEI along with two voltage tracking controllers were proposed and developed for energy efficient DC to AC power conversion. The system performance was evaluated in terms of stability, system dynamics, switching loss and THD and validated

via simulation. Using a simple output filter the output voltage THD was limited within 0.2% which fulfills IEEE 519. Utilizing the mixed input voltage to the inverter generated by bidirectional buck converter, the total switching loss of the proposed two-stage PEI is almost half that of the one-stage PEI. Moreover, the robust voltage and current control performance can be guaranteed even under varied load impedance and output power variations.

CHAPTER 4

LEARNING BACKSTEPPING CONTROLLER

The pulse width modulated (PWM) voltage-source inverters (VSIs) have been more broadly utilized for DC to AC voltage conversion as emerging technologies such as inverter-based Distributed Generation (DG), Vehicle to Grid (V2G), Battery Energy Storage System (BESS) and Uninterruptable Power Supplies (UPS) are more widely adopted.

On the hand, the nonlinearity of residential electrical load is steadily increasing with the growing use of devices such as computers, fax machines, printers, refrigerators, TVs and electronic lighting ballasts, with rectifier at their front end. This nonlinearity of the load deviates both current and voltage waveform in the distribution feeder from its sinusoidal waveform. As such designing an inverter system with a nonlinear controller that can take into account this nonlinearity in the load current and generate a sinusoidal output voltage has become of great interest in applications where a high quality voltage is needed. Another metric in the performance evaluation of inverters is a fast transient response during load change which also necessitates the use of high performance controllers. Several control schemes have been proposed for the control of an inverter with an output LC to reduce the aberrance of inverter source's output voltage waveform including adaptive bank

resonant filters [59], deadbeat control [60], [16] and multiloop feedback control [15] [14]. In [61], Internal Model Theory was adopted, and a traditional PI control scheme combined with repetitive controller was applied to manage the inverter system. But the model was not applicable for nonlinear loads. In [36] a Fuzzy control strategy was used to control the inverter system, with a genetic algorithm used in conjunction to optimize the fuzzy controller. In [19] a combination of repetitive control and state-feedback-with-integral control was proposed to control the output voltage waveform of the inverter. The schemes presented in [36] and [19] have an acceptable dynamic response and output voltage waveform even with nonlinear load at the cost of a complex algorithm. In [38] the performance of a backstepping controller in control of a single phase inverter with resistive load is compared with that of sliding mode and conventional PID controller. The results reveal that the backstepping controller outperforms the other two controllers in terms of both transient response and steady state error. Also it is shown that the sliding mode controller generates a very harsh command compared to backstepping. In previous chapter a backstepping controller was proposed for the control of H-Bridge inverter with a very good tracking performance demonstrated. The work presented in previous chapter uses a Backstepping controller combined with a sliding technique to compensate the unmeasurable uncertainties arose from the derivative of the output current. It was also assumed that the system experience a constant disturbance.

In this chapter a backstepping controller combined with a periodic learning scheme is proposed for the control of an H-Bridge inverter with output LC filter in the presence of a nonlinear load [62]. The proposed learning scheme take into account the periodic nature of the system and observes the periodic disturbance and unmeasurable uncertainties of the

system. A Lyapunov stability analysis is presented which proves that the sinusoidal voltage tracking objective is achieved by the controller with all signals remaining bounded. Simulation results further validate this approach.

4.1 System Model

An H-Bridge inverter with a LC output filter is used for DC to AC power conversion. The inverter is sourcing four different type of loads, including linear and nonlinear loads, as seen in Fig. 4.1. Applying the state averaging method, and unipolar PWM switching scheme the average model for the H-Bridge inverter can be written as follows [47]:

$$C\dot{V}_o = I_L - I_o \tag{4.1}$$

$$L\dot{I}_L = V_{in}(D + d) - RI_L - V_o \tag{4.2}$$

where L, C, R are the inductance, capacitance and series resistance of the inductance, respectively. $V_{in}(t) \in \mathbb{R}$ is the input supply voltage, $D(t) \in$[-1 1] is the PWM duty ratio and d is the periodic PWM disturbance resulted from imperfect PWM switching timing. $V_o(t) \in \mathbb{R}$, $I_o(t) \in \mathbb{R}$ and $I_L(t) \in \mathbb{R}$ are the output voltage, output current and the inductor current, respectively. To facilitate the control development, the following assumptions are made.

Assumption 1: L, C, R, V_{in} are known, constant system parameters.

Assumption 2: The output voltage $V_o(t)$, inductor current $I_L(t)$, and output current $I_o(t)$ are measurable.

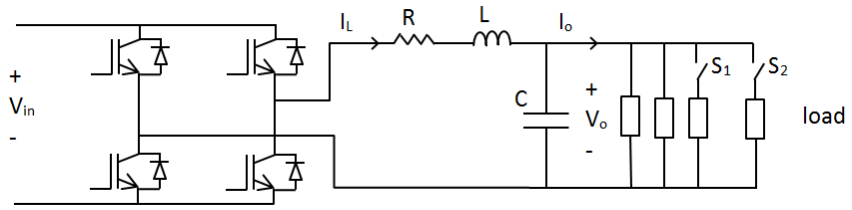

Fig. 5.1 H-Bridge inverter with output LC filter and load.

Assumption 3: The load current has the following properties: $I_o, \dot{I}_o(t) \epsilon \mathcal{L}_\infty$, so that $L\left|\dot{I}_o(t)\right| < \beta_1$.

Assumption 4: The desired voltage and its first and second derivatives with respect to time are bounded, $V_d(t), \dot{V}_d(t), \ddot{V}_d(t) \in \mathcal{L}_\infty$.

Assumption 5: The periodic disturbance *d* is bounded, $|d| < \beta_2$.

4.2 Control System Development

The objective of the control scheme is to design $D(t)$ such that $V_o(t) \rightarrow V_d(t)$ as $t \rightarrow \infty$, where $V_d(t)$ is the sinusoidal output voltage trajectory defined by desired amplitude, frequency, and phase.

4.2.1 Error System Development

In order to meet the desired voltage, tracking error signal $e(t) \in \mathbb{R}$ and auxiliary error signal $\eta(t) \in \mathbb{R}$ are defined as:

$$e \triangleq V_d - V_o \tag{4.3}$$

$$\eta \triangleq I_d - I_L \tag{4.4}$$

where $\mathrm{I_d(t)} \in \mathbb{R}$ is an auxiliary control signal which will be designed subsequently. Taking derivative of both sides of equations (4.3) and (4.4), pre-multiplying by L and C,

respectively, and then utilizing equations (4.1) and (4.2) gives the following open loop error system:

$$C\dot{e} = C\dot{V}_d - I_d + \eta + I_o \tag{4.5}$$

$$L\dot{\eta} = L\dot{I}_d - V_{in}D - V_{in}d + RI_L + V_o \tag{4.6}$$

4.2.2 Control Input Design

The control inputs will be designed based on the mathematical form of (4.5) and (4.6) along with the subsequently presented stability analysis. The auxiliary control signal $I_d(t)$ is designed as follows

$$I_d \triangleq C\dot{V}_d + K_1 e + I_o \tag{4.7}$$

where $K_1 \in \mathbb{R}^+$ is a positive control gain. Examining the form of (4.6) we see that reduction of the error equation to a desirable closed loop form requires compensation of the term $\dot{I}_d(t)$. From (4.7), we see that $\dot{I}_d(t)$ includes the term $\dot{I}_o(t)$.

$$L\dot{\eta} = L\dot{I}_o - V_{in}D - V_{in}d + W_1 \tag{4.8}$$

where :

$$W_1 \triangleq LC\ddot{V}_d + LK_1\dot{V}_d - \frac{LK_1}{C}(I_L - I_o) + RI_L + V_o. \tag{4.9}$$

While a numerical derivative of the output current, $\dot{I}_o(t)$, is possible to calculate, taking the derivative of a noisy current measurement is not a practical solution. Therefore our approach will consider this term as a periodic disturbance. Thus a new term d_1 is introduced which contains all of the lumped system disturbances.

$$d_1 \triangleq L\dot{I}_o - V_{in}d \tag{4.10}$$

Motivated by the subsequent stability analysis the duty ratio control signal, $D(t)$, is defined as :

$$D \triangleq \frac{1}{V_{in}}\left[W_1 + e + K_2\eta + \hat{d}_1\right] \tag{4.11}$$

where $K_2 \in \mathbb{R}^+$ is a positive control gain and $\hat{d}_1$ is an observation of the system disturbances, d_1, which is developed in the following subsection.

4.2.3 Periodic Learning Design

Considering the fact that in an AC system the PWM disturbance, output current and consequently its derivative with respect to time are periodic, a periodic learning method is developed to estimate the system disturbances defined in (4.10). To characterize the performance of the learning scheme the following error signal is defined.

$$\tilde{d}_1 \triangleq d_1 - \hat{d}_1 \tag{4.12}$$

Motivated by subsequent stability analysis the following update law is defined for periodic learning of d_1.

$$\hat{d}_1(t) \triangleq Sat_\beta\left(\hat{d}_1(t-T)\right) + K_3\eta(t) \tag{4.13}$$

where $\beta > \beta_1 + \beta_2$ is a system constant, and $Sat_\beta(.)$ is a saturation function with upper and lower limits equal to β and $-\beta$, respectively. $K_3 \in \mathbb{R}^+$ is a positive control gain and T is the period of the AC system. Substituting (4.13) into (4.12) and considering the fact that $d_1(t)$ is periodic and bounded, $d_1 < \beta$, the learning error can be given by:

$$\tilde{d}_1(t) = d_1(t) - \hat{d}_1(t) = d_1(t-T) - \hat{d}_1(t)$$
$$= Sat_\beta\big(d_1(t-T)\big) - Sat_\beta\left(\hat{d}_1(t-T)\right) - K_3\eta \tag{4.14}$$

Substituting (4.7), (4.10), (4.11) and (4.12) into the open loop error systems from (4.5) and (4.8) results in the following closed loop error systems.

$$C\dot{e} = -K_1 e + \eta \tag{4.15}$$

$$L\dot{\eta} = -e - K_2\eta + \tilde{d}_1 \tag{4.16}$$

4.2.4 Stability Analysis

Theorem 1: Using the closed loop error system equations found in (4.15) and (4.16), the error signals defined in (4.3) and (4.4) are regulated as follows

$e(t), \hat{\eta}(t) \to 0 \; as \; t \to \infty$.

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined by equation (4.17).

$$S = \frac{1}{2}Ce^2 + \frac{1}{2}L\eta^2 + \frac{1}{2K_3}\int_{t-T}^{T}\left[Sat_\beta\big(d_1(\tau)\big) - Sat_\beta\left(\hat{d}_1(\tau)\right)\right]^2 d\tau \tag{4.17}$$

Taking the derivative of (4.17) with respect to time and substituting the closed loop error signals from (4.15) and (4.16) and applying Leibniz rule, the expression in (4.18) is obtained.

$$\dot{S} = -K_1e^2 - K_2\eta^2 + \eta\tilde{d}_1 + \frac{1}{2K_3}\left[Sat_\beta\big(d_1(t)\big) - Sat_\beta\left(\hat{d}_1(t)\right)\right]^2$$
$$-\frac{1}{2K_3}\left[Sat_\beta\big(d_1(t-T)\big) - Sat_\beta\left(\hat{d}_1(t-T)\right)\right]^2. \tag{4.18}$$

Substituting (4.14) into (4.18) the following equation for $\dot{S}(t)$ can be obtained.

$$\dot{S} = -K_1 e^2 - K_2 \eta^2 - \frac{1}{2K_3}\left[\tilde{d}_1 + K_3\eta\right]^2 + \eta\tilde{d}_1 + \frac{1}{2K_3}\left[Sat_\beta\left(d_1(t)\right) - Sat_\beta\left(\hat{d}_1(t)\right)\right]^2 \tag{4.19}$$

Substituting for $\tilde{d}_1(t)$ from(4.12), after some mathematical simplifications (4.19) can be rewritten as:

$$\dot{S} = -K_1 e^2 - (K_2 + \frac{K_3}{2})\eta^2 + \frac{1}{2K_3}\left[\left(Sat_\beta\left(d_1(t)\right) - Sat_\beta\left(\hat{d}_1(t)\right)\right)^2 - \left(d_1(t) - \hat{d}_1(t)\right)^2\right] \tag{4.20}$$

The last term of (4.20) can be upper bounded as follows:

$$\left(Sat_\beta\left(d_1(t)\right) - Sat_\beta\left(\hat{d}_1(t)\right)\right)^2 - \left(d_1(t) - \hat{d}_1(t)\right)^2 \leq 0 \tag{4.21}$$

Using (4.21) $\dot{S}(\mathrm{t})$ can be upper bounded as:

$$\dot{S} \leq -K_1 e^2 - (K_2 + \frac{K_3}{2})\eta^2 \tag{4.23}$$

From the structure of (4.23) it can be proved that all signals are bounded and $e(t), \eta(t) \to 0$ as $t \to \infty$. From (4.17) and (4.23) it is clear that $e(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ [63]. From (4.3) and the fact that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_o(t) \in \mathcal{L}_\infty$. From (4.7) along with Assumption 3 and 4 it is clear that $I_d(t) \in \mathcal{L}_\infty$. From (4.15) and $e(t), \eta(t) \in \mathcal{L}_\infty$ it is clear that $\dot{e}(\mathrm{t}) \in \mathcal{L}_\infty$. From the definition of $Sat_\beta(.)$ function and $\eta(t) \in \mathcal{L}_\infty$, using (4.13) we can deduce that $\hat{d}_1(t) \in \mathcal{L}_\infty$. Since $I_d(t), \eta(t) \in \mathcal{L}_\infty$ from (4.4) it is obvious that $I_L(t) \in \mathcal{L}_\infty$. Now from (4.9) and (4.11) along with $\ddot{V}_d(t), \dot{V}_d(t), V_o(t), I_L(t), I_o(t), e(t), \eta(t),$

$\hat{d}_1(t) \in \mathcal{L}_\infty$ it is clear that $D(t) \in \mathcal{L}_\infty$. From (4.12) and $\hat{d}_1(t) \in \mathcal{L}_\infty$ along with Assumption 5 it is clear that $\tilde{d}_1 \in \mathcal{L}_\infty$. From (4.16) we can see that $\dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$. Hence it is clear that all signals in the closed loop are bounded. Since $e(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t), \dot{\eta}(t) \in \mathcal{L}_\infty$, Barbalat's Lemma [49] can be utilized to prove that $e(t), \eta(t) \rightarrow 0 \ as \ t \rightarrow \infty$. Thus completing the proof of the theorem.

4.3 Simulation Results

To validate the periodic learning observer and control design a numerical simulation was performed under various load scenarios. The Matlab-Simulink computer simulation software with PLECS Blockset was used to model the circuit dynamics of the inverter and the control schemes. Table 4.1 summarizes all the parameters used for the inverter circuit and the control scheme simulation. This table also includes the parameters of four different loads denoted as Load1, …, Load4 used in the simulation. The desired voltage trajectory was selected to be $V_d = 220\sqrt{2}sin(2\pi 50t)$. The inverter's operation begins at t = 0[s] while sourcing a complex load, Load1, and a nonlinear load, Load 2. The nonlinear load is a rectifier with output capacitor and a resistive load. In order to simulate changes in the system load , a complex load, Load 3, and a nonlinear load, Load 4, are switched into the circuit at t=0.092[s] and 0.132[s], respectively.

The output voltage and current of the inverter are demonstrated in Fig. 2. As it can be seen in this figure the proposed controller generates an almost pure sinusoidal output voltage in the presence of a nonlinear output current waveform. Fig. 3 shows the controller

Table 4.1 System Parameters for H-Bridge Inverter and Learning Backstepping Controller

	Parameter	Value	Units		Parameter	Value	Units
Inverter	L	500	µH		V_{in}	360	V
	C	330	µF		k_1	10	-
	R	0.3	Ω		k_2	50	-
	f	50	Hz		k_3	50	-
	V_o	220	V(rms)		β	20	-
Loa	P_1	3	kW	Loa	P_3	2	kW
	Q_1	1.45	kVar		Q_3	1	kVar
Loa	P_2	800	W	Loa	P_4	500	W

tracking performance in terms of the output voltage tracking error, $e(t)$, and inductor current tracking error, $\eta(t)$. Fig. 4 shows the generated duty ratio control signal, $D(t)$. The actual and desired inductor current are shown in Fig. 5 and the estimated system disturbance is demonstrated in Fig 6.

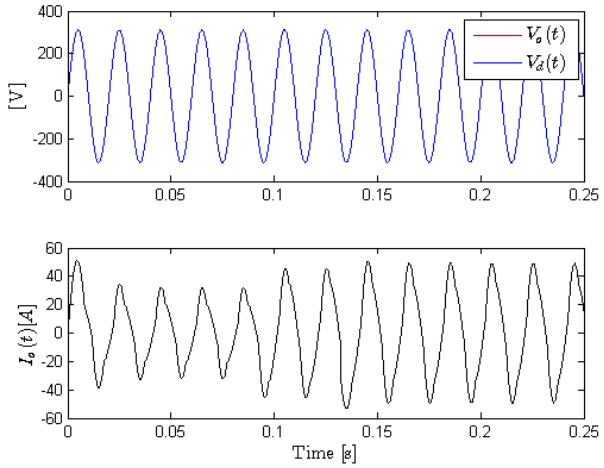

Fig. 4. 2 Inverter desired voltage, output voltage and output current.

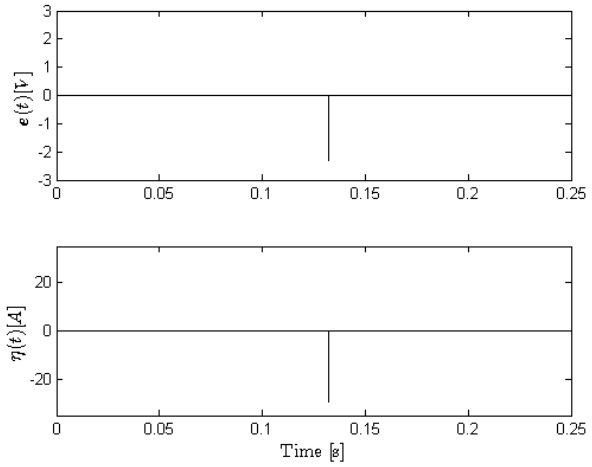

Fig. 4. 3 Controller tracking errors.

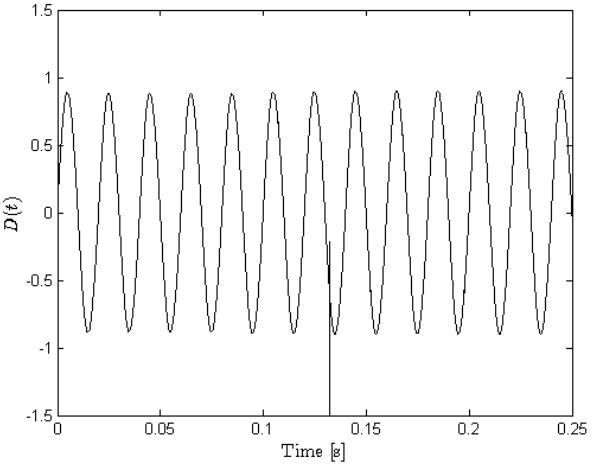

Fig. 4. 4 Inverter control duty cycle.

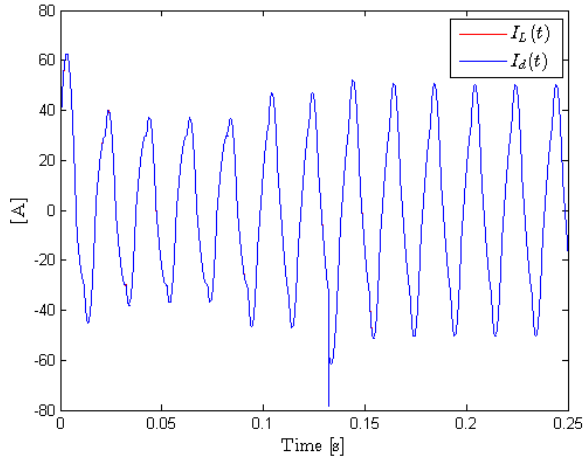

Fig. 4. 5 Actual and desired current of the inductor.

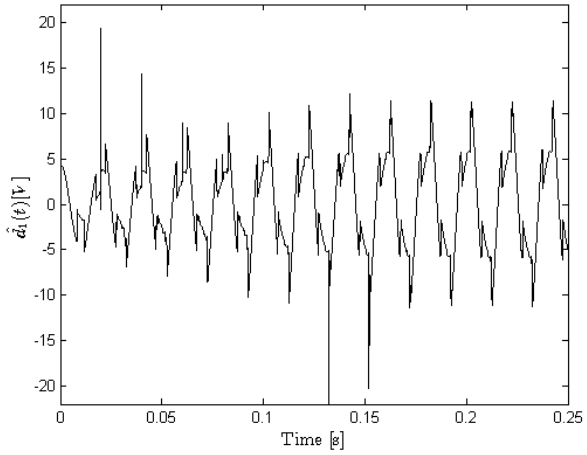

Fig. 4. 6 Estimation of system disturbances.

In Assumption 3, it is assumed that the output current is continuous, i.e. that $\left|\dot{I}_o(t)\right| \in \mathcal{L}_\infty$. However, in the case of momentary violation of this assumption during step changes in the load the controllers still perform acceptably. The system behavior for the load changes can be seen at t=0.092[s] and 0.132[s]. Sudden change of system load resulting from the addition of an inductive complex load at t=0.092[s] does not degrade the system

performance in terms of tracking errors depicted in Fig 3. That is because this load change does not violate the aforementioned assumptions. However the addition of a nonlinear rectifier load with output capacitor initial voltage equal to zero at t=0.112[s] results in a discontinuity in output current and consequently violates Assumption 3. Although this violation causes a deviation in the error signals from zero, the fast dynamic response of the controller compensates for this deviation and the controller error signals converge to zero very quickly. These load changes introduce deviations to the estimated disturbance at the corresponding times and these deviations repeats at the subsequent cycles because of the periodic nature of the learning scheme. The amplitude of deviations diminish in subsequent cycles as the learning algorithm re-convergences. From these figures it is clear that the closed loop controlled inverter works well within the desired parameters, achieving a pure sinusoidal output voltage.

4.4 Summary

A backstepping control scheme along with a periodic learning observer were developed for an H-Bridge inverter with output LC filter sourcing both linear and nonlinear loads. The system performance was evaluated in terms of tracking performance and stability. These schemes have been validated by both stability analysis and simulation results and all these analysis and simulations have demonstrated the effectiveness of the proposed control solution.

CHAPTER 5

BACKSTEPPING CONTROLLER FOR 3-PHASE INVERTER WITH SEAMLESS TRANSITION TO GRID-TIE

Three-phase inverters with output LC filters are commonly employed for generation of sinusoidal output voltage with low harmonic distortion, suitable for distributed generation systems. However, the waveform quality of the output voltage in stand-alone mode is poor under the nonlinear load using conventional controllers. This issue has become more pressing as the nonlinearity of the load current in power systems continues to increase due to the growing number of electronic devices with rectifiers at the front end of their power supply present in the grid. As such, designing a nonlinear controller that can account for the nonlinearities of the load current to generate a high quality output voltage has become of great interest.

In the two previous chapters, two controllers utilizing backstepping technique were developed for a single phase inverter in abc-frame. The difficulty with developing a backstepping controller for a 3-phase inverter in abc- frame is the need for synthesis of desired AC trajectories and their first and second order derivatives. This problem becomes more difficult especially when there is a need for amplitude, phase and frequency adjustment in transition from standalone to grid-tie mode.

In this chapter a backstepping controller developed in $dq0$-frame is proposed for the control of a 3-phase 4-wire diode clamped inverter with output LC filter under different loads including balanced, unbalanced, linear and nonlinear loads [64]. In addition, an observer is developed for load-current estimation, enhancing the behavior of the proposed controller especially for the cases that there is a need to remove the costly output current sensor. Also, the seamless transition of the inverter from standalone to grid-tie is investigated while the inverter is under the control of the proposed controller. Lyapunov stability analysis and simulation results validate the effectiveness of the proposed control solution in terms of tracking objective and in meeting the THD requirements of IEEE 519 and EN 50160 standards for US and European power systems, respectively.

5.1 System Model

In this work we consider a 3-level 3-leg (3L3L) diode clamped inverter with split dc bus connected to a three phase load, as seen in Fig. 5.1. This topology can be used to feed both balanced/unbalanced Δ or Y type load with or without a neutral conductor. Although the controller can be developed in any frame, the rotating *dq0*-frame is selected for the following reasons.

First, as we will see in the proceeding controller development, the backstepping controller requires the synthesis of a desired voltage trajectory, and its first and second time derivatives. In the *dq0*-frame this trajectory can be represented by a constant value making it and its derivatives much easier to synthesize than the AC signals required in abc-frame or $\alpha\beta$-frame.

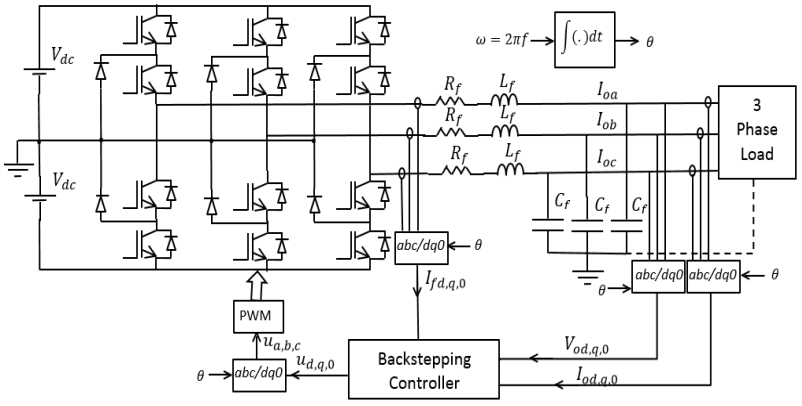

Fig. 5. 1 3L3L four-wire diode clamped inverter with output *LC* filter.

Second, transition from two operational modes: standalone to grid-tied, can be accomplished much easier in the dq0-frame.

Applying the state averaging method and using the well-known Park's Transformation, the equivalent $dq0$ circuits of the system model are shown in Fig. 5.2 where $\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix}$ are the $dq0$ transformation of the control input (duty ratio) $\begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix}$ in abc-frame.

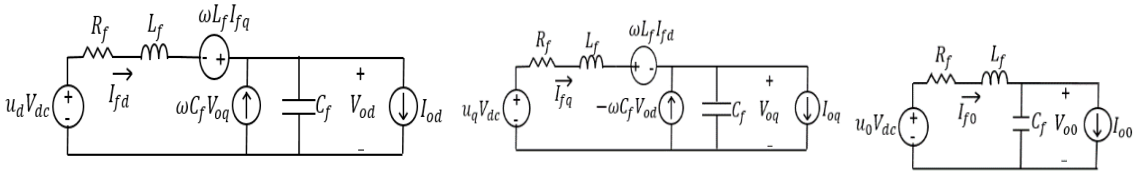

Fig. 5. 2 Equivalent *dq0* circuits of the 3L3L diode clamped inverter with output *LC* filter.

From the system model in *dq0*-frame shown in Fig. 5.2, the system equations can be written as follows:

$$C_f \dot{V}_{od} = I_{fd} + \omega C_f V_{oq} - I_{od} \tag{5.1}$$

$$L_f \dot{I}_{fd} = (u_d + u'_d)V_{dc} - R_f I_{fd} + \omega L_f I_{fq} - V_{od} \tag{5.2}$$

$$C_f \dot{V}_{oq} = I_{fq} - \omega C_f V_{od} - I_{oq} \tag{5.3}$$

$$L_f \dot{I}_{fq} = \left(u_q + u'_q\right)V_{dc} - R_f I_{fq} - \omega L_f I_{fd} - V_{oq} \tag{5.4}$$

$$C_f \dot{V}_{o0} = I_{f0} - I_{o0} \tag{5.5}$$

$$L_f \dot{I}_{f0} = (u_0 + u'_0)V_{dc} - R_f I_{f0} - V_{o0} \tag{5.6}$$

where L_f, C_f, R_f are the inductance, capacitance and series resistance of the inductance of the filter, respectively. $V_{dc} \in \mathbb{R}$ is the split DC-link voltage and $\begin{bmatrix} u'_d \\ u'_q \\ u'_0 \end{bmatrix}$ are the transformation of the PWM disturbance resulting from imperfect PWM switching timing. The system frequency, ω in [rad/s], is related to the reference angle for the Park's Transformation as follows:

$$\theta = \int_{t_0}^{t} \omega(\tau) + \theta_0. \tag{5.7}$$

5.2 Control System Development

The objective of the control scheme is to design $\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix}$ such that $\begin{bmatrix} V_{od} \\ V_{oq} \\ V_{o0} \end{bmatrix} \rightarrow \begin{bmatrix} V_{rd} \\ V_{rq} \\ V_{r0} \end{bmatrix} \rightarrow$ as $t \rightarrow \infty$ where $\begin{bmatrix} V_{rd} \\ V_{rq} \\ V_{r0} \end{bmatrix}$ is the reference voltage trajectory. If this control objective is met then the

inverse Park's Transformation can be used to convert the control signals $\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix}$ from $dq0$-frame to abc-frame, to generate the desired 3 phase voltage trajectory. This requires synchronization of the frequency and phase of the reference angle, θ, to match the desired frequency and phase.

Because of the coupling of the signals in the d and q axis, the controller for these two axes are developed together. Development of the controller in the zero axis can be inferred from the developed controller for the other two axes by simply substituting $\omega = 0$.

To facilitate the control development, the following assumptions are made.

Assumption 1: L_f, C_f, R_f, V_{dc} are known, constant system parameters.

Assumption 2: The output voltage, output current and inductor current are measurable.

Assumption 3: The load current has the following properties:

$I_{od}(t), \dot{I}_{od}(t), I_{oq}(t)$, and $\dot{I}_{oq}(t) \in \mathcal{L}_\infty$.

Assumption 4: The disturbance $\begin{bmatrix} u'_d \\ u'_q \\ u'_0 \end{bmatrix}$ are bounded and slowly time-varying in comparison to the switching dynamics in the sense that $\begin{bmatrix} \dot{u}'_d \\ \dot{u}'_q \\ \dot{u}'_0 \end{bmatrix} \approx \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$.

Assumption 5: The reference voltage trajectory and its first and second derivatives with respect to time in *dq0*-frame are bounded, $V_{rd}(t), \dot{V}_{rd}(t), \ddot{V}_{rd}(t), V_{rq}(t), \dot{V}_{rq}(t), \ddot{V}_{rq}(t) \in \mathcal{L}_\infty$.

If the reference frame is intended to be synchronized with the reference AC voltage trajectory with amplitude of V_{peak} then $V_{rd} = V_{peak}$ and $V_{rq} = 0$. Consequently, we have:

$$\dot{V}_{rd}(\mathrm{t}) = \ddot{V}_{rd}(\mathrm{t}) = \dot{V}_{rq}(t) = \ddot{V}_{rq}(t) = 0.$$

5.2.1 Error System Development

In order to meet the desired voltage, tracking error signals $e_d(t), e_q(t) \in \mathbb{R}$ are defined as:

$$e_d \triangleq V_{rd} - V_{od} \tag{5.8}$$

$$e_q \triangleq V_{rq} - V_{oq}. \tag{5.9}$$

To proceed with the control development, we will define auxiliary error signals $\eta_d(t), \eta_q(t) \in \mathbb{R}$ as:

$$\eta_d \triangleq I_{rd} - I_{fd} \tag{5.10}$$

$$\eta_q \triangleq I_{rq} - I_{fq} \tag{5.11}$$

where $I_{rd}, I_{rq} \in \mathbb{R}$ are auxiliary control signals which will be designed subsequently. Taking the derivative of (5.8) and substituting the values of $\dot{V}_{od}$ and I_{fd} from (5.1) and (5.10) the following open loop error equation is obtained:

$$C_f \dot{e_d} = C_f \dot{V}_{rd} - I_{rd} + \eta_d - \omega C_f V_{oq} + I_{od}. \tag{5.12}$$

Moreover , taking the derivative of (5.10) and substituting for $\dot{I}_{fd}$ from (5.2) we get:

$$L_f \dot{\eta_d} = L_f \dot{I}_{rd} - (u_d + u_d')V_{dc} - \omega L_f I_{fq} \tag{5.13}$$

$$+R_f I_{fd} + V_{od}.$$

In the same manner, working with equations (5.9) and (5.11) we get:

$$C_f \dot{e_q} = C_f \dot{V}_{rq} - I_{rq} + \eta_q + \omega C_f V_{od} + I_{oq} \tag{5.14}$$

$$\begin{aligned} L_f \dot{\eta_q} = L_f \dot{I}_{rq} - \left(u_q + u_q'\right) V_{dc} + \omega L_f I_{fd} \\ +R_f I_{fq} + V_{oq} \end{aligned} \tag{5.15}$$

5.2.2 Control Design

The control inputs will be designed based on the mathematical form of (5.12)-(5.15) along with the subsequently presented stability analysis. The auxiliary control signals I_{rd} found in (5.12) is designed as follows:

$$I_{rd} \triangleq C_f \dot{V}_{rd} - \omega C_f V_{oq} + I_{od} + K_{1d} e_d \tag{5.16}$$

where $K_{1d} \in \mathbb{R}^+$is a positive control gain. The control law defined in (5.16) is substituted into (5.12) so the following closed loop error system for $e_d(t)$ is obtained.

$$C_f \dot{e_d} = -K_{1d} e_d + \eta_d \tag{5.17}$$

Taking time derivative of (5.16) and substituting into (5.13) after some mathematical simplifications results in:

$$L_f \dot{\eta}_d = F_d + L_f \dot{I}_{od} - u_d V_{dc} - (\hat{u}_d' + \tilde{u}_d') V_{dc} \tag{5.18}$$

where $F_d(t)$ is an expression equal to:

$$F_d \triangleq L_f C_f \ddot{V}_{rd} + L_f K_{1d} \dot{V}_{rd} - \omega L_f I_{fq} + R_f I_{fd} + V_{od}$$
$$- \frac{L_f K_{1d}}{C_f} \left[I_{fd} + \omega C_f V_{oq} - I_{od} \right] \tag{5.19}$$
$$- L_f \omega (I_{fq} - \omega C_f V_{od} - I_{oq})$$

and $\hat{u}'_d$ is the estimated disturbance with the following estimation error and update law:

$$\tilde{u}'_d \triangleq u'_d - \hat{u}'_d \tag{5.20}$$

$$\dot{\hat{u}}'_d \triangleq -K_{4d} \eta_d V_{dc} \tag{5.21}$$

where $K_{4d} \in \mathbb{R}^+$is a positive gain. From (5.18) and motivated by the subsequent stability analysis the duty ratio control signal, u_d, is defined as :

$$u_d \triangleq \frac{1}{V_{dc}} [F_d + e_d + K_{2d} \eta_d + K_{3d} sgn(\eta_d)] - \hat{u}'_d \tag{5.22}$$

where $sgn(.)$ is the sign function of the error η_d ,and $K_{2d}, K_{3d} \in \mathbb{R}^+$are positive control gains. Substituting (5.22) into (5.18) provides the following closed loop error system for $\eta_d(t)$

$$L_f \dot{\eta}_d = L_f \dot{I}_{od} - e_d - K_{2d} \eta_d - K_{3d} sgn(\eta_d) - \tilde{u}'_d V_{dc}. \tag{5.23}$$

Following the same procedure, we get the following equations for the q axis. The auxiliary control signals I_{rq} found in (5.14) is designed as follows:

$$I_{rq} \triangleq C_f \dot{V}_{rq} + \omega C_f V_{od} + I_{oq} + K_{1q} e_q \tag{5.24}$$

where $K_{1q} \in \mathbb{R}^{+}$is a positive control gain. Substituting the control law defined in (5.24) into (5.14), we obtain the following closed loop error system for e_q.

$$C_f \dot{e_q} = -K_{1q} e_q + \eta_q \tag{5.25}$$

Substituting the time derivative of (5.24) into (5.15), after some mathematical simplifications results in:

$$L_f \dot{\eta}_q = F_q + L_f \dot{I}_{oq} - u_q V_{dc} - \left(\hat{u}_q' + \tilde{u}_q'\right) V_{dc} \tag{5.26}$$

where $F_q(t)$ is defined by:

$$\begin{aligned} F_q \triangleq\ & L_f C_f \ddot{V}_{rq} + L_f K_{1q} \dot{V}_{rq} + \omega L_f I_{fd} + R_f I_{fq} + V_{oq} \\ & - \frac{L_f K_{1q}}{C_f} \left[I_{fq} - \omega C_f V_{od} - \ I_{oq} \right] \\ & + L_f \omega \left(I_{fd} + \omega C_f V_{oq} - I_{od} \right). \end{aligned} \tag{5.27}$$

The estimation error, $\tilde{u}_q'$, and update law for the estimated disturbance, $\hat{u}_q'$, is defined as:

$$\tilde{u}_q' \triangleq u_q' - \hat{u}_q' \tag{5.28}$$

$$\dot{\hat{u}}_q' \triangleq -K_{4q} \eta_q V_{dc} \tag{5.29}$$

where $K_{4q} \in \mathbb{R}^{+}$is a positive gain. The structure of (5.26) along with the subsequent stability analysis motivate the duty ratio control signal, u_q, to be defined as :

$$u_q \triangleq \frac{1}{V_{dc}} \left[F_q + e_q + K_{2q} \eta_q + K_{3q} sgn(\eta_q) \right] - \hat{u}_q' \tag{5.30}$$

where $K_{2q}, K_{3q} \in \mathbb{R}^{+}$are positive control gains. Eventually the closed loop error system for $\eta_q$is obtained as follows.

$$L_f\dot{\eta}_q = L_f\dot{I}_{oq} - e_q - K_{2q}\eta_q - K_{3q}sgn(\eta_q) - \tilde{u}_q' V_{dc} \tag{5.31}$$

5.2.3 Stability Analysis

Theorem 1: Using the closed loop error system equations found in (5.17), (5.23), (5.25) and (5.31), respectivley the error signals defined in (5.8)-(5.11) are regulated as follows:

$$e_d(t), e_q(t), \eta_d(t), \eta_q(t) \to 0 \; as \; t \to \infty$$

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined as follows.

$$\begin{aligned} S \triangleq & \frac{1}{2}C_f e_d^2 + \frac{1}{2}C_f e_q^2 + \frac{1}{2}L_f \eta_d^2 + \frac{1}{2}L_f \eta_q^2 \\ & + \frac{1}{2K_{4d}}\tilde{u}_d'^{\,2} + \frac{1}{2K_{4q}}\tilde{u}_q'^{\,2} \end{aligned} \tag{5.32}$$

Taking the derivative of (5.32) with respect to time and substituting the closed loop error signals from (5.17), (5.23), (5.25) and (5.31) after some mathematical simplifications, the expression (5.33) is obtained where (5.21) and (5.29) are also utilized.

$$\begin{aligned} \dot{S} = & -K_{1d}e_d^2 - K_{1q}e_q^2 - K_{2d}\eta_d^2 - K_{2q}\eta_q^2 \\ & + \eta_d L_f \dot{I}_{od} - K_{3d}|\eta_d| + \eta_q L_f \dot{I}_{oq} - K_{3q}|\eta_q| \end{aligned} \tag{5.33}$$

The expression in (5.34) can be upper bounded as follows:

$$\begin{aligned} \dot{S} \leq & -K_{1d}e_d^2 - K_{1q}e_q^2 - K_{2d}\eta_d^2 - K_{2q}\eta_q^2 \\ & + |\eta_d|(L_f|\dot{I}_{od}| - K_{3d}) + |\eta_q|(L_f|\dot{I}_{oq}| - K_{3q}) \end{aligned} \tag{5.34}$$

Assuming that the control gains are selected as stated in (5.35) and (5.36), then (5.34) can be further simplified as (5.37).

$$K_{3d} \geq L_f \left| \dot{I}_{od} \right| \tag{5.35}$$

$$K_{3q} \geq L_f \left| \dot{I}_{oq} \right| \tag{5.36}$$

$$\dot{S} \leq -K_{1d} e_d^2 - K_{1q} e_q^2 - K_{2d} \eta_d^2 - K_{2q} \eta_q^2 \tag{5.37}$$

From (5.32) and (5.37) it is clear that $e_d, e_q, \eta_d, \eta_q \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\tilde{u}'_d, \tilde{u}'_q \in \mathcal{L}_\infty$. From (5.8), (5.9) and the fact that $V_{rd}, V_{rq} \in \mathcal{L}_\infty$, therefore $V_{od}, V_{oq} \in \mathcal{L}_\infty$. From (5.16), (5.24) along with Assumption 3 and 5 it is clear that $I_{rd}, I_{rq} \in \mathcal{L}_\infty$, so from (5.10), (5.11) we can deduce that $I_{fd}, I_{fq} \in \mathcal{L}_\infty$. From (5.17), (5.25) and $e_d, e_q, \eta_d, \eta_q \in \mathcal{L}_\infty$ it is clear that $\dot{e_d}, \dot{e_q} \in \mathcal{L}_\infty$. Since $\tilde{u}'_d, \tilde{u}'_q \in \mathcal{L}_\infty$ and considering Assumption 4, from (5.20), (5.28) we can deduce that $\hat{u}'_d, \hat{u}'_q \in \mathcal{L}_\infty$. From (5.22), (5.30) we can see that all the signals contributed in the definition of u_d, u_q are bounded, therefore $u_d, u_q \in \mathcal{L}_\infty$. Considering Assumption 3 and 5, from (5.23), (5.31) we can deduce that $\dot{\eta}_d,\ \dot{\eta}_q \in \mathcal{L}_\infty$. Hence it is clear that all signals in the closed loop are bounded. Since $e_d, e_q, \eta_d, \eta_q \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e_d}, \dot{e_q}, \dot{\eta}_d,\ \dot{\eta}_q \in \mathcal{L}_\infty$ Barbalat's Lemma [13] can be utilized to prove that $e_d(t), e_q(t), \eta_d(t), \eta_q(t) \to 0$ as $t \to \infty$. Thus completing the proof of the theorem.

5.2.4 Variable Gain Control

As it can be seen in (5.22) and (5.30), a sliding technique comprising the sign of errors multiplied with a constant gain, $K_{3d} sgn(\eta_d)$ and $K_{3q} sgn(\eta_q)$, are used to compensate for the uncertainty presented by derivative of the output current appeared in (5.23) and (5.31). While the stability of the system necessitates a large value for the gains, (5.22) and (5.30)

show a large value of K_{3d} and K_{3q} generates a very harsh command. To alleviate this issue, a variable gain controller is proposed as follows:

$$K_{3x} = \begin{cases} k_{3x} & If\ |e_x(t)| > e_{th} \\ \alpha k_{3x} & If\ |e_x(t)| \leq e_{th} \end{cases} \tag{5.38}$$

where $x \in \{d, q, 0\}$ can be any axis in $dq0$-frame, k_{3x} is a positive gain and $\alpha \ll 1$ is a reduction factor. As can be inferred from (5.38), at the transient time or at the moment that the system experiences a sudden change in the system load which increases the system error above a predefined threshold, e_{th}, a higher gain, k_{3x} is used to keep the system stable. Meanwhile in the steady state operation of the system this gain is reduced by factor of α to alleviate the generation of the hard command.

5.3 Output Current Observer

To eliminate the need for a costly current sensor to measure the output current, an observer is developed in this subsection. In the observer developed in this section the derivative of the observed current is calculated as part of update law, which can be used to compensate for the numerical derivative of the output current in the associate control development. This fact can resolve the problem of hard command arose from sliding control presented in previous section.

A simple observation of the load current can be calculated from (5.1), and (5.3) through inductor current and output voltage measurement. However, the required numerical derivative would make such an observation very sensitive to noise. In a PWM-VSI the switching and sampling frequency are typically orders of magnitude higher than

the fundamental frequency. Therefore, in comparison with the sampling and switching frequencies, the current is changing very slowly, so that it can be approximated as a constant [14].

$$L_f \dot{I}_{od} = 0 \tag{5.39}$$

$$L_f \dot{I}_{oq} = 0 \tag{5.40}$$

The following observer errors can be used to evaluate the observer performance.

$$\tilde{I}_{od} = I_{od} - \hat{I}_{od} \tag{5.41}$$

$$\tilde{I}_{oq} = I_{oq} - \hat{I}_{oq} \tag{5.42}$$

With the assumptions presented in (5.39) and (5.40) we have:

$$\dot{\hat{I}}_{od}(t) = -\dot{\tilde{I}}_{od} \tag{5.43}$$

$$\dot{\hat{I}}_{oq}(t) = -\dot{\tilde{I}}_{oq} \tag{5.44}$$

Following the same procedure as previous section and substituting $I_{od}$and $I_{oq}$from (5.41) and (5.42) respectively, an open loop error system is developed as follows

$$C_f \dot{e_d} = C_f \dot{V}_{rd} - I_{rd} + \eta_d - \omega C_f V_{oq} + \hat{I}_{od} + \tilde{I}_{od}. \tag{5.45}$$

$$\begin{aligned} L_f \dot{\eta_d} = {} & L_f \dot{I}_{rd} - (u_d + u'_d) V_{dc} - \omega L_f I_{fq} \\ & + R_f I_{fd} + V_{od}. \end{aligned} \tag{5.46}$$

$$C_f \dot{e_q} = C_f \dot{V}_{rq} - I_{rq} + \eta_q + \omega C_f V_{od} + \hat{I}_{oq} + \tilde{I}_{oq} \tag{5.47}$$

$$L_f\dot{\eta}_q = L_f\dot{I}_{rq} - \left(u_q + u_q'\right)V_{dc} + \omega L_f I_{fd} + R_f I_{fq} + V_{oq} \tag{5.48}$$

In the same manner, the auxiliary control signals, I_{rd} and I_{rq}, and the duty ratio control signal, u_d and u_q, are designed as follows:

$$I_{rd} \triangleq C_f\dot{V}_{rd} - \omega C_f V_{oq} + \hat{I}_{od} + K_{1d}e_d \tag{5.49}$$

$$I_{rq} \triangleq C_f\dot{V}_{rq} + \omega C_f V_{od} + \hat{I}_{oq} + K_{1q}e_q \tag{5.50}$$

$$u_d \triangleq \frac{1}{V_{dc}}[F_d + e_d + K_{2d}\eta_d] - \hat{u}_d' \tag{5.51}$$

$$u_q \triangleq \frac{1}{V_{dc}}\left[F_q + e_q + K_{2q}\eta_q\right] - \hat{u}_q' \tag{5.52}$$

where $F_d(t)$ and $F_q(t)$ are expressions equal to:

$$F_d \triangleq L_f C_f\ddot{V}_{rd} + L_f K_{1d}\dot{V}_{rd} - \omega L_f I_{fq} + R_f I_{fd} + V_{od} - \frac{L_f K_{1d}}{C_f}\left[I_{fd} + \omega C_f V_{oq} - \hat{I}_{od}\right] - L_f\omega(I_{fq} - \omega C_f V_{od} - \hat{I}_{oq}) + L_f\dot{\hat{I}}_{od} \tag{5.53}$$

$$F_q \triangleq L_f C_f\ddot{V}_{rq} + L_f K_{1q}\dot{V}_{rq} + \omega L_f I_{fd} + R_f I_{fq} + V_{oq} - \frac{L_f K_{1q}}{C_f}\left[I_{fq} - \omega C_f V_{od} - \hat{I}_{oq}\right] + L_f\omega\left(I_{fd} + \omega C_f V_{oq} - \hat{I}_{od}\right) + L_f\dot{\hat{I}}_{oq}. \tag{5.54}$$

Substituting (5.49)-(5.52) in open loop errors, (5.45)-(5.48), results in the following close loop error system.

$$C_f \dot{e_d} = -K_{1d} e_d + \eta_d + \tilde{I}_{od} \tag{5.55}$$

$$L_f \dot{\eta}_d = -e_d - K_{2d} \eta_d - \tilde{u}'_d V_{dc} + \frac{L_f K_{1d} \tilde{I}_{od}}{C_f} \tag{5.56}$$

$$C_f \dot{e_q} = -K_{1q} e_q + \eta_q + \tilde{I}_{oq} \tag{5.57}$$

$$L_f \dot{\eta}_q = -e_q - K_{2q} \eta_q - \tilde{u}'_q V_{dc} + \frac{L_f K_{1q} \tilde{I}_{oq}}{C_f} \tag{5.58}$$

Motivated by subsequent stability analysis the update law for the unknown load current is defined as:

$$\dot{\hat{I}}_{od} \triangleq K_{5d}(e_d + \tfrac{L_f K_{1d}}{C_f} \eta_d) \tag{5.59}$$

$$\dot{\hat{I}}_{oq} \triangleq K_{5q}\left(e_q + \frac{L_f K_{1q}}{C_f} \eta_q\right). \tag{5.60}$$

And consequently:

$$\hat{I}_{od} = \int_{t_0}^{t} K_{5d}(e_d(\tau) + \tfrac{L_f K_{1d}}{C_f} \eta_d(\tau))\, d\tau + \hat{I}_{od}(t_0) \tag{5.61}$$

$$\hat{I}_{oq} = \int_{t_0}^{t} K_{5q}(e_q(\tau) + \tfrac{L_f K_{1d}}{C_f} \eta_q(\tau))\, d\tau + \hat{I}_{oq}(t_0) \tag{5.62}$$

where $K_{5d}$and K_{5d} are positive gains.

5.3.1 Stability Analysis

Theorem 2: Using the closed loop error system equations found in (5.55)-(5.58) the error signals defined in (5.8)-(5.11) are regulated as follows:

$$e_d(t), e_q(t), \eta_d(t), \eta_q(t) \to 0 \; as \; t \to \infty$$

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined as follows.

$$\begin{aligned} S \triangleq & \frac{1}{2} C_f e_d^2 + \frac{1}{2} C_f e_q^2 + \frac{1}{2} L_f \eta_d^2 + \frac{1}{2} L_f \eta_q^2 \\ & + \frac{1}{2K_{4d}} \tilde{u}_d'^{\,2} + \frac{1}{2K_{4q}} \tilde{u}_d'^{\,2} \\ & + \frac{1}{2} K_5^{-1} \tilde{I}_{od}^2 + \frac{1}{2} K_5^{-1} \tilde{I}_{od}^2 \end{aligned} \tag{5.63}$$

Taking the derivative of (5.63) with respect to time and substituting the closed loop error signals from (5.55)-(5.58) after some mathematical simplifications, the expression (5.64) is obtained where (5.21), (5.29), (5.59) and (5.60) are also utilized.

$$\dot{S} = -K_{1d} e_d^2 - K_{1q} e_q^2 - K_{2d} \eta_d^2 - K_{2q} \eta_q^2 \tag{5.64}$$

From the structure of (5.63) and (5.64) in the same maner as presented in previous section, it can be proved that all signals are bounded and

$$e_d(t), e_q(t), \eta_d(t), \eta_q(t) \to 0 \; as \; t \to \infty.$$

5.4 Transition from Standalone to Grid-Tie

For a seamless transition from standalone to grid-tie, the magnitude of the inverter output voltage should match that of the grid voltage and the inverter need to be synchronized with the grid as well. Since the voltage amplitude, V_{peak}, in abc-frame is equal to the voltage on d-axis of the $dq0$-frame, so the inverter voltage amplitude can simply be adjusted by setting $V_{rd} = V_{peak}$. A proper change of $V_{rd}$is through a

differentiable function which does not violate Assumption 5. Although the step change of V_{rd}violates Assumption 5, the effect of this momentary violation will be diminished after the step time depending on the transient response of the controller.

For the synchronization, the frequency and phase of the inverter output voltage should match those of the grid. To this end, the reference angle for the Park's transformation and inverse Park's transformation, θ, should be synchronized with the recovered phase of a PLL locked on the grid voltage. Fig. 5.3 shows the block diagram of a circuit that can be used for reference angle generation. In this figure f_r is the reference frequency. For the frequency adjustment $f_r$can be selected to match the grid frequency measured by the PLL. For the phase adjustment, a rectangular signal with area of integration equal to the phase difference between the grid voltage and the inverter voltage can be applied to the phase adjustment input of the circuit. For example, if the grid voltage leads the inverter voltage $\Delta\varphi$ [rad/s], then a rectangular signal with amplitude of A and duration of Δt[s] which are related to $\Delta\varphi$ with the following equation can be used to adjust the inverter phase during Δt second. Fig. 5.4 shows the overall system block diagram.

$$A\Delta t = \Delta\varphi \tag{5.65}$$

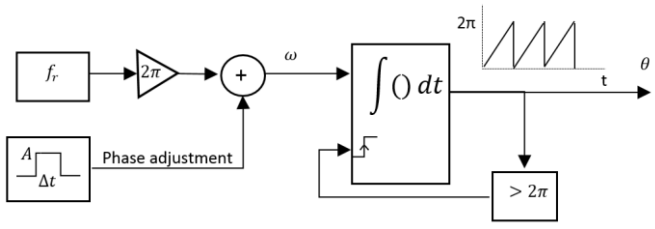

Fig. 5.3 Reference angle generator.

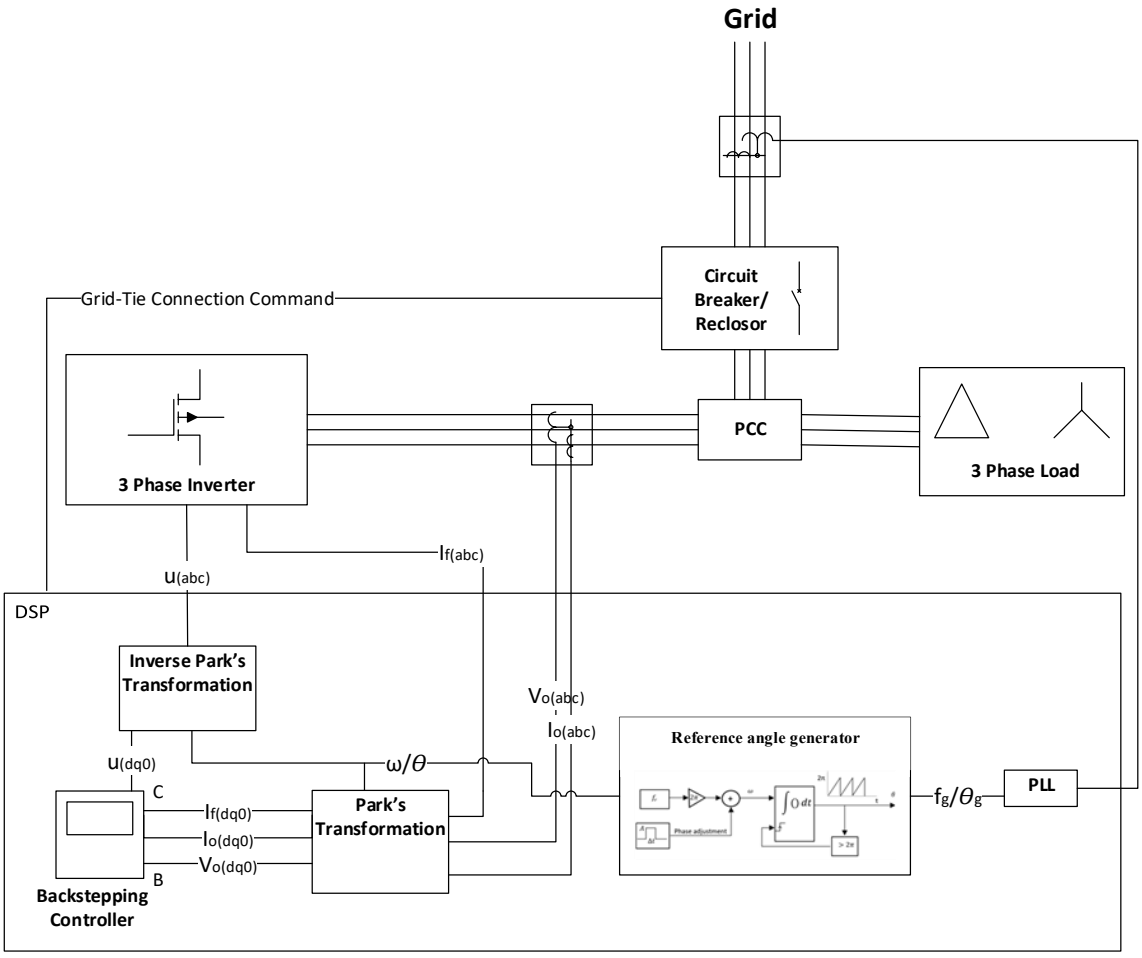

Fig. 5.4 Overall system block diagram.

5.5 Simulation Result

To validate the control design a numerical simulation was performed. The PLECS toolbox is used with Matlab/Simulink to model the instantaneous circuit dynamics of the inverter and the control schemes. The parameters used for the inverter circuit and the control scheme are summarized in Table 5.1. The performance of the proposed control scheme is evaluated under various scenarios including, unbalanced load, nonlinear load

and transition from standalone to grid-tie. The simulation results are presented for a 3-wire delta connected load. With inherent neutral point of the 3L3L inverter as shown in Fig. 5.1, the feasibility to control a 4-wire wye connected load is obvious.

Table 5.1 System Parameters for 3-Phase Inverter

	Parameter	Value	Units	Gain	Value
Inverter	L_f	300	µH	K_{1d}	10
	C_f	330	µF	K_{2d}	10
	R_f	0.4	Ω	k_{3d}	1000
	f_{sw}	60	kHz	K_{4d}	1
	f_r	60	Hz	K_{5d}	100
	$V_{DC} = 2 * V_{dc}$	2*270	V	K_{1q}	10
	V_o	120	V (rms)	K_{2q}	1
Load 1	P_1	12	kW	k_{3q}	1000
	Q_1	6	kVar	K_{4q}	1
Load 2	P_2	2	kW	K_{5q}	100
	Crest Factor	2:1		α	0.03
	e_{th}	3	V		

5.5.1 Unbalanced Load

The inverter is initially feeding a balanced delta type inductive load, Load1. This load becomes unbalanced by decreasing the load impedance connected to the phase a and b by half at t= 0.08[s]. Fig. 5.5 shows the inverter performance under balanced and unbalanced load in both abc and $dq0$ frames. As it can be seen in this figure the imbalance between the load current of different phases manifests as mixed (AC+DC) signals in the $dq0$-frame representation of the output current. The controller tracking performance is demonstrated

in Fig. 5.6 in terms of output voltage and inductor current tracking errors. The signals in this figure are zoomed to show both transient and steady state error. From these figures it is clear that the closed loop controlled inverter works well within the desired parameters under both balanced and unbalanced load, achieving a pure sinusoidal output voltage.

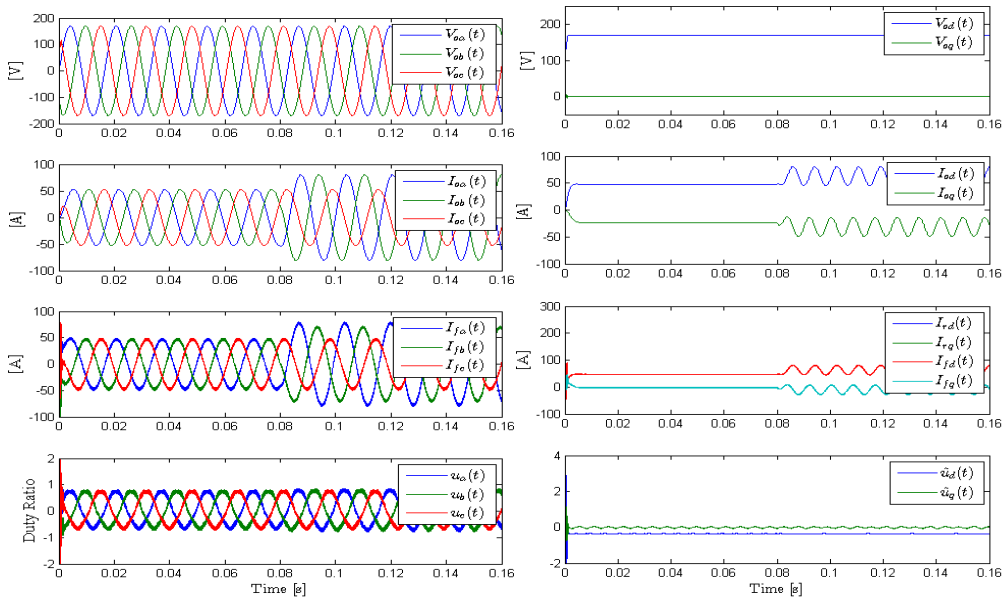

Fig. 5.5 Inverter performance under balanced/unbalanced load.

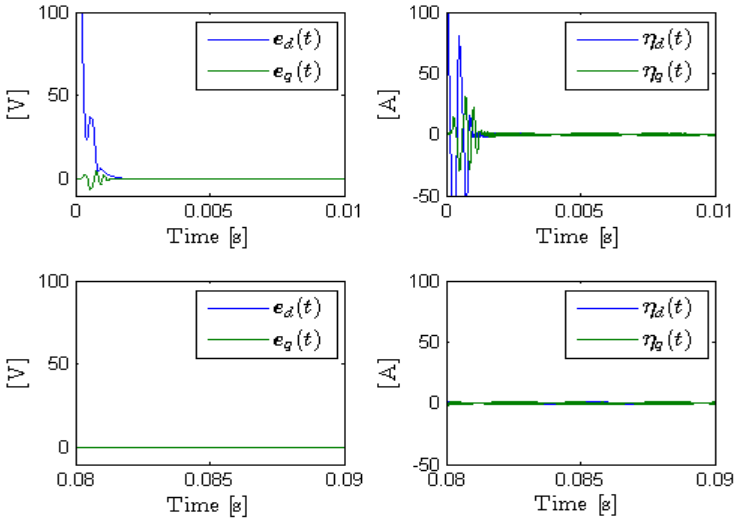

Fig. 5.6 Tracking error under balanced/unbalanced load.

5.5.2 Nonlinear Load

The nonlinear load, Load2, is a rectifier with output capacitor and a resistive load. To evaluate the system performance under nonlinear load, Load2 is switched into the circuit at t=0.08[s] while the system was initially feeding Load1.

The inverter performance under nonlinear load in both abc and $dq0$ frames is shown in Fig. 5.7. This figure shows that the nonlinearity of the load current results in adding nonlinear waveform to the dc signal representing the output current in $dq0$-frame. Fig. 5.8 demonstrates the tracking performance in terms of output voltage and inductor current tracking errors. In Assumption 3, it is assumed that the output current is continuous, $\dot{I}_{od}(t), \dot{I}_{oq}(t) \in \mathcal{L}_\infty$. However, in the case of momentary violation of this assumption during step changes in the load the controllers still perform acceptably. The system behavior for the load changes can be seen at t=0.08[s]. Addition of a nonlinear rectifier load with output capacitor initial voltage equal to zero results in a discontinuity in output current and consequently violates Assumption 3 and gain conditions (5.35) and (5.36). Although this violation causes a deviation in the error signals, the fast dynamic response of the controller compensates for this deviation and the controller error signals converge very quickly. From these figures it is clear that the closed loop controlled inverter works well within the desired parameters under nonlinear load, achieving a pure sinusoidal output voltage. Table 5.2 gives the individual voltage distortion for the first five harmonics of the inverter output voltage. As it can be seen, the individual voltage distortion is less than 0.03% which meets the harmonic limits of the IEEE 519 ($< 3\%$) and EN 50160($<$ 0.5%). The total harmonic distortion of output voltage is 0.17 % which fulfills total voltage distortion limits of IEEE 519 (THD < 5%) and EN 50160 (THD < 8 %).

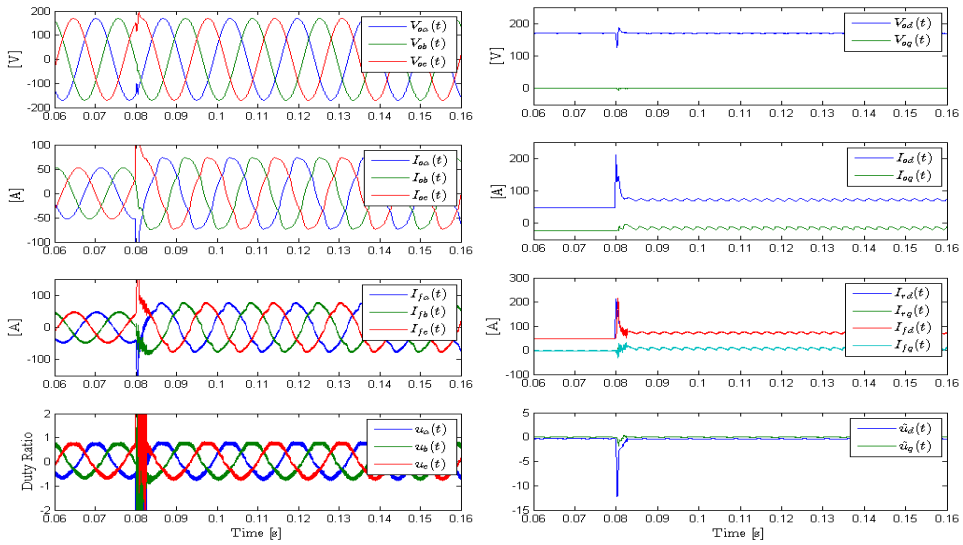

Fig. 5.7 Inverter performance under nonlinear load.

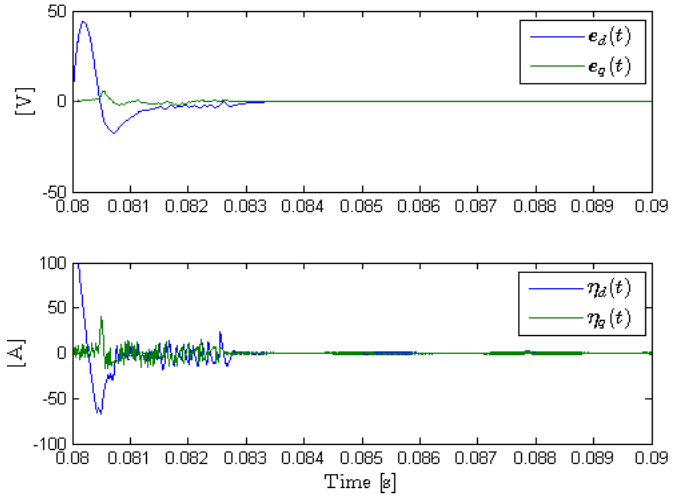

Fig. 5.8 Tracking error under nonlinear load.

Table 5.2 Harmonic Distortions

n	Distortion	
	Unbalanced Load	Nonlinear Load
2	0.03%	0.02%
3	4.2×10^{-3}%	3.4×10^{-3}%
4	0.03%	0.03%
5	3.2×10^{-3}%	0.02%
THD	0.17%	0.17%

5.5.3 Transition from Standalone to Grid-tie

For a seamless transition from standalone to grid-tie, the amplitude, frequency and phase of the inverter should be changed to match those of the grid. Although all of these changes can be accomplished simultaneously, in the simulation each of them is performed in a specific time to evaluate the performance of the controller in response to each change. Fig. 5.9 shows the line-to-line voltage of grid and inverter in transition from standalone to grid-tie. At t=0.05 [s], the desired amplitude of the inverter phase voltage, V_{rd}, changes from $120\sqrt{2}$ to $115\sqrt{2}$. As it was pointed out in previous section, this step change of V_{rd}violates Assumption 5. Although this violation causes a deviation in the error signals, as shown in Fig. 5.11 the fast dynamic response of the controller compensates for this deviation and the controller error signals converge very quickly.

At t=0.06 [s], the reference frequency of the inverter changes from 60 [Hz] to 60.5 [Hz] with a ramp function with the slope of 100 [Hz/s] to match the grid frequency measured by a PLL. At t=0.07[s] the grid and inverter output voltage are $180°$ out of phase. The phase adjustment is made by applying a rectangular waveform from t=0.7 [s] to t=0.9 [s] with $\Delta t = 0.02$[s] and $A = \pi/0.02$ [rad/s] to the Phase adjustment input of circuit

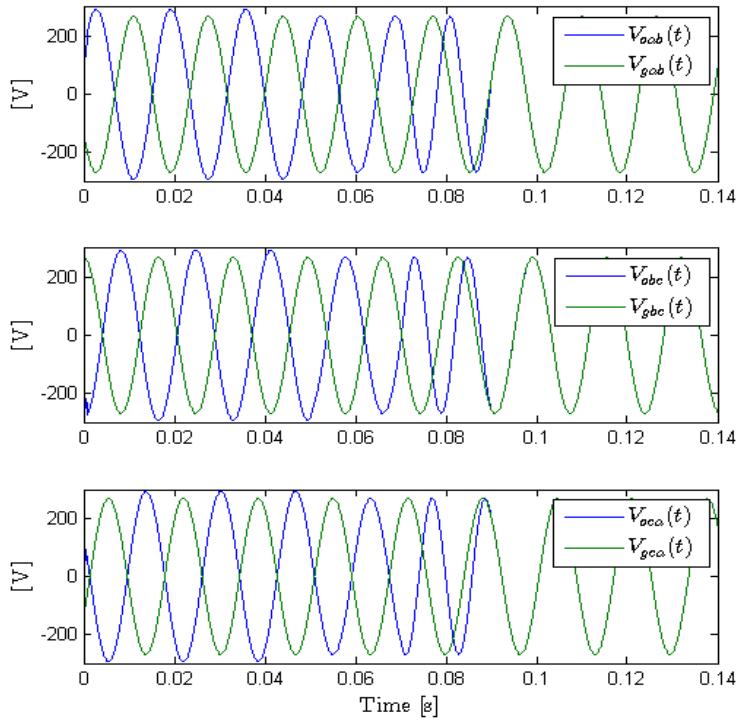

Fig. 5.9 Line-to-line voltage of inverter and grid in transition from standalone to grid-tie.

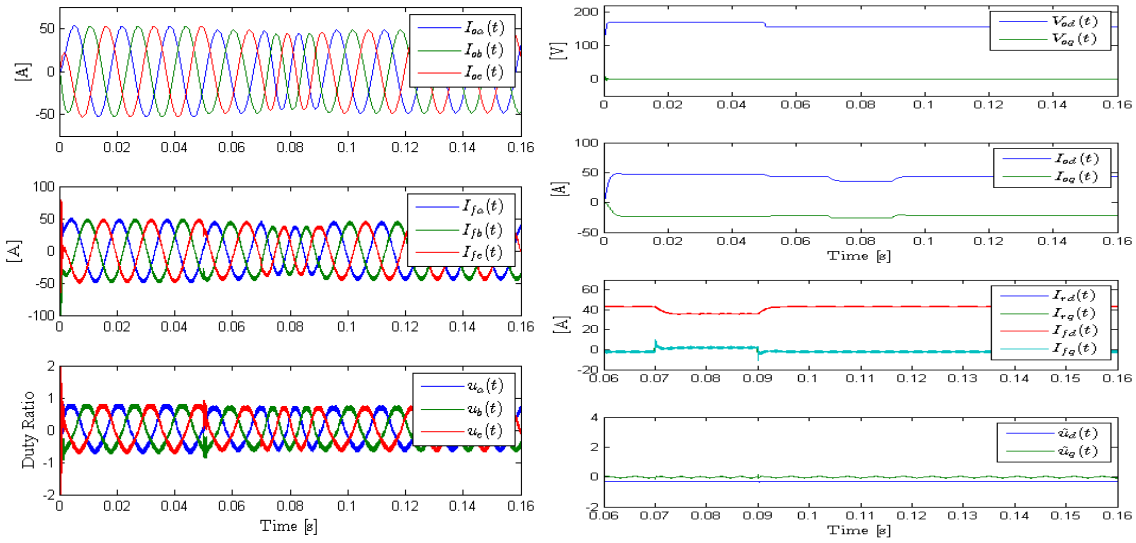

Fig. 5.10 Inverter performance in transition from standalone to grid-tie.

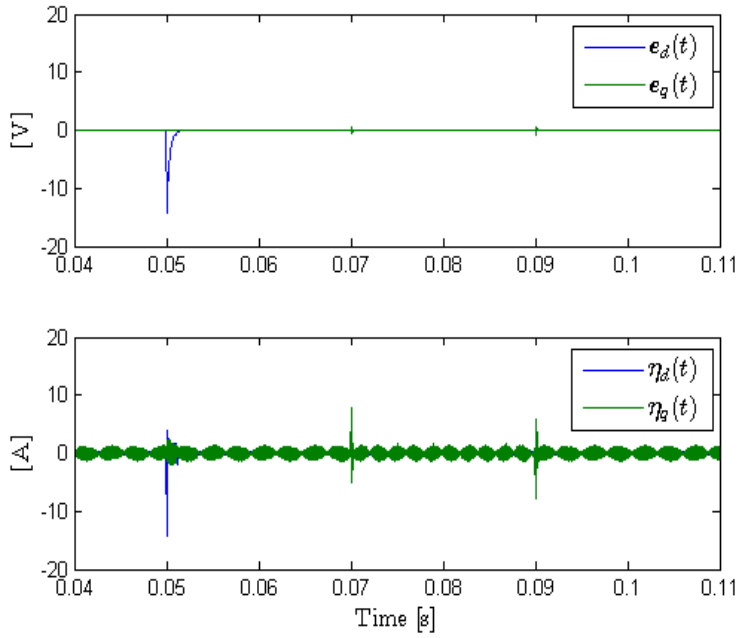

Fig. 5.11 Tracking error in transition from standalone to grid-tie.

demonstrated in Fig. 5.3. As it can be seen in Fig. 5.11, these frequency and phase adjustments do not affect the controller performance in terms of tracking error. At t=0.1[s] a circuit breaker/recloser connects the inverter to the grid. As it can be inferred from Fig. 5.10 and 5.11 this transition is seamless without any discontinuities in the output voltage and current.

5.5.4 Output Current Observer

Fig. 5.12 and 5.14 show the performance of the inverter with backstepping controller and output current observer under unbalanced and nonlinear loads, respectively. The controller tracking performance is demonstrated in Fig. 5.13 and 5.15 in terms of output voltage and inductor current tracking errors. Again, in the case of sudden load change, see Fig. 5.14 and 5.15, a deviation in the error signals arises which will be compensated with fast dynamic response of the controller.

Comparing the duty ratio control command signals for the backstepping controller combined with a load-current observer depicted in Fig. 5.12 and 5.14, with those of the backstepping controller combined with sliding technique, depicted in Fig. 5.5 and 5.7, it can be seen that the former has a less harsh control command at the cost of greater steady state errors (Compare Fig. 5.6 and 5.8 with Fig. 5.13 and 5.15, respectively).

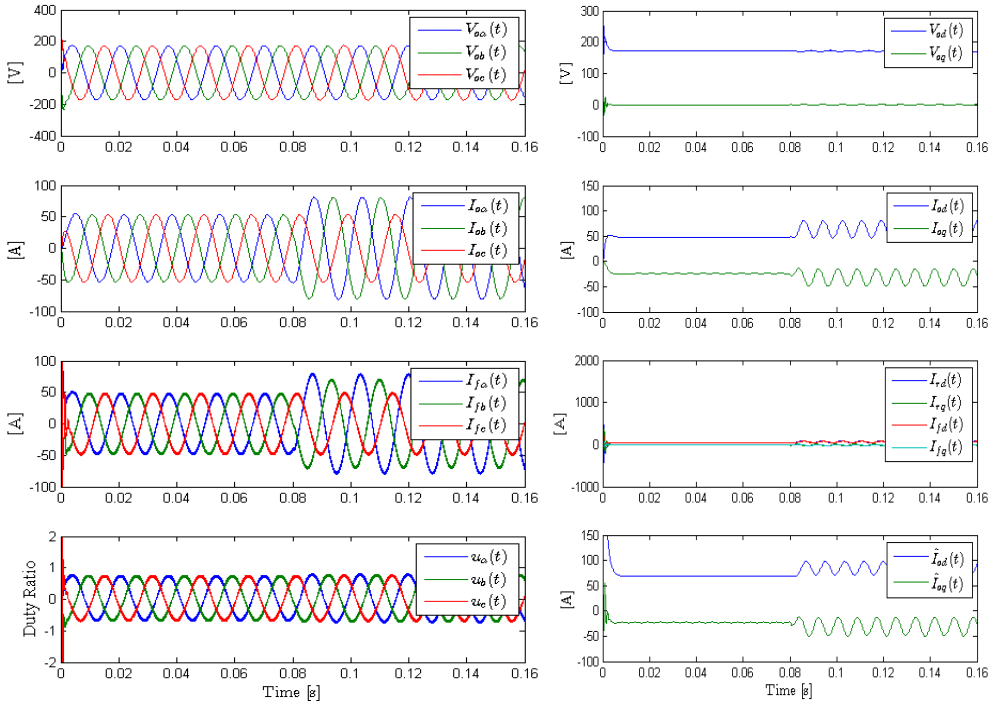

Fig. 5.12 Inverter performance with load-current observer under balanced/unbalanced load.

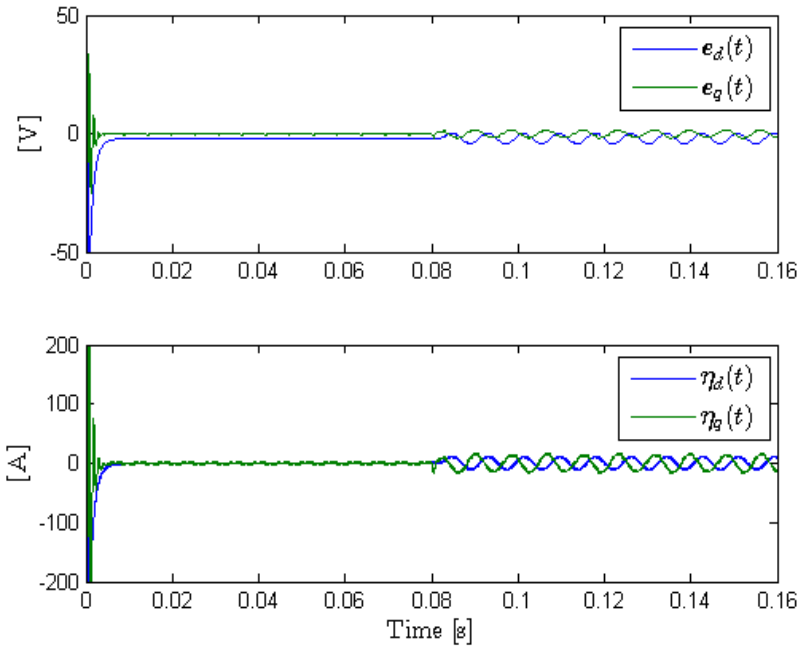

Fig. 5.13 Tracking error with load-current observer under balanced/unbalanced load.

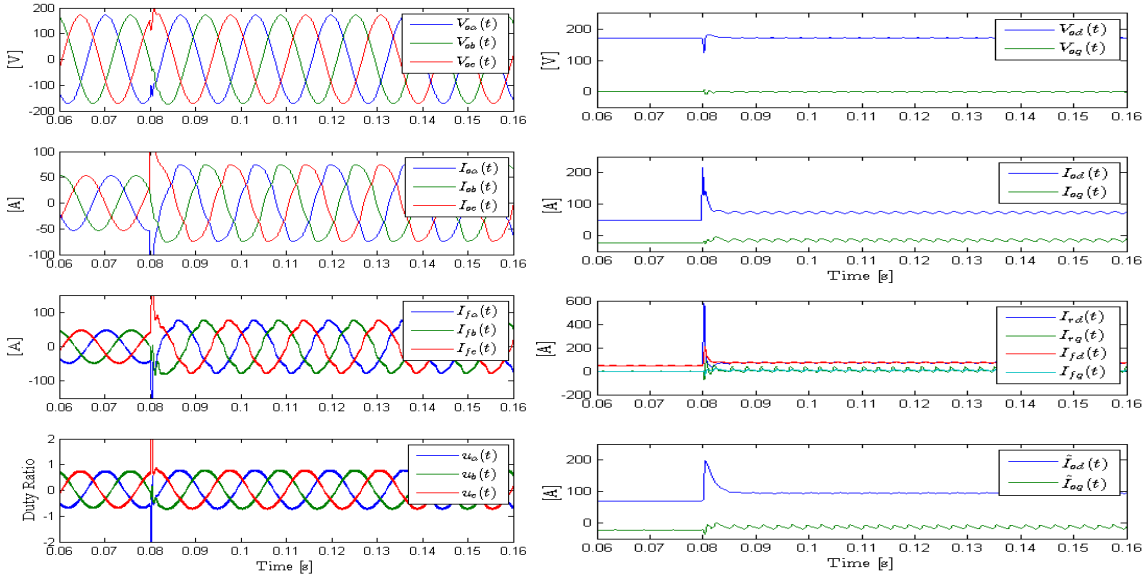

Fig. 5.14 Inverter performance with load-current observer under nonlinear load.

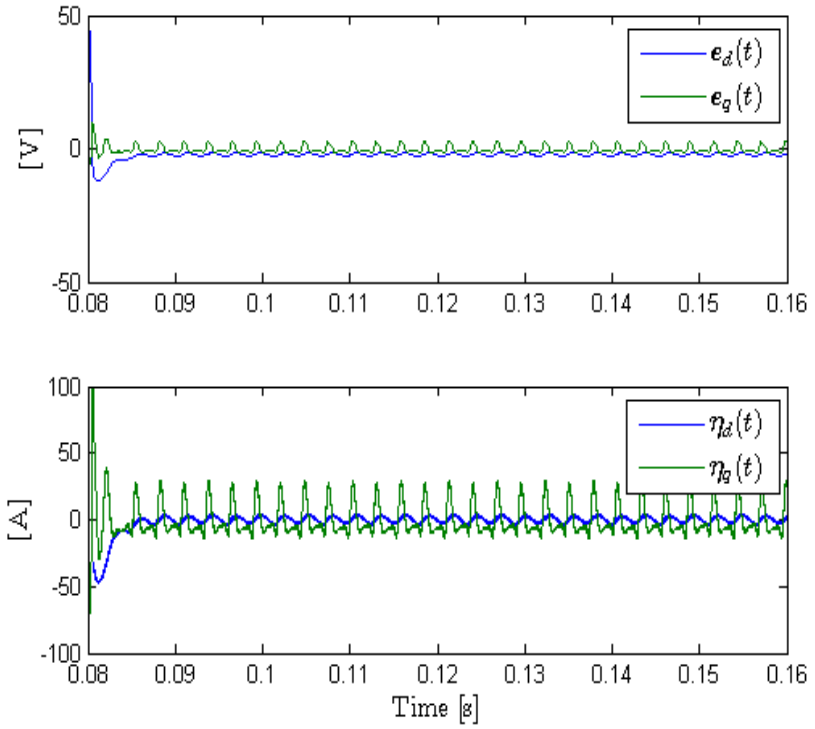

Fig. 5.15 Tracking error with load-current observer under nonlinear load.

5.6 Summary

In this chapter a backstepping control scheme was developed for a 3-phase 4-wire diode clamped inverter with output *LC* filter sourcing a variety of load including balanced, unbalanced, linear and nonlinear loads. The proposed controller is developed in $dq0$-frame with a feasible dc trajectory for the output signal. Also development of the controller in this frame results in a scheme for seamless transition from standalone to grid-tie mode. The system behavior was enhanced with using variable gain technique and combining the proposed controller with a load-current observer. The system performance is evaluated in terms of tracking performance, stability, system dynamics, and THD and validated via simulation and analysis. All these analysis and simulations have demonstrated the effectiveness of the proposed control solution. Using a simple *LC* output filter the output

voltage THD was limited within 0.17% which fulfills IEEE 519 and EN 50160 for US and European power systems, respectively.

CHAPTER 6

A BACKSTEPPING CONTROLLER COMBINED WITH INDUCTOR CURRENT AND OUTPUT CURRENT OBSERVERS

In this chapter, a backstepping controller combined with two novel current observers is proposed for the control of a single-phase H-Bridge inverter [65]. As it was mentioned earlier in the Introduction section this control law is applicable for any converter/inverter in the class of buck-type converters. The control laws of the proposed backstepping and sliding mode controllers in [38] depend on the numerical derivative of the output current which increase the level of the noise in the system. In [57] and Chapter 3 a backstepping controller is proposed for the control of H-Bridge inverter with a nonlinear load with a very good tracking performance demonstrated. In the control schemes presented in [38] and [57], two sensors are used to measure output voltage and current in addition to another current sensor for the inductor current. In practice this inductor current measurement has a significant amount of ripple resulting from PWM switching. This ripple is then propagated into the control algorithm adding disturbance to the system.

In this chapter a backstepping controller combined with two novel nonlinear observers are presented to eliminate the need for costly current sensors to measure the inductor current and the output current. Furthermore, because this observed inductor current is based

off of the cycle average model of the VSI the aforementioned ripple is not present in the signal. Also, in the proceeding output current observer development an observation for the derivative of output current is achieved which eliminates the need for a noise-sensitive numerical derivative such as that utilized in [38]. The elimination of the sensors along with the elimination of current ripple and noise provides an advantage over previous methods. A Lyapunov stability analysis is presented which proves that the voltage tracking objective is achieved by the controller with all signals remaining bounded. Simulation results further validate this approach by demonstrating sinusoidal output voltage tracking even under a highly distorting nonlinear load.

6.1 System Model

An H-Bridge inverter with a simple LC output filter as seen in Fig. 6. 1 is used for DC to AC power conversion. Applying the state averaging method, and unipolar PWM switching scheme the average model for an H-Bridge inverter can be written as follows [47]:

$$L\dot{I}_L = V_{in}D - RI_L - V_o \tag{6.2}$$

$$C\dot{V}_o = I_L - I_o \tag{6.2}$$

where L, C, R are the inductance, capacitance and series resistance of the inductance, respectively. $V_{in}$is the input supply voltage, $D(t)$ is the PWM duty ratio and $I_L(t)$ is the inductor current. $V_o(t)$, and $I_o(t)$ are the output voltage and output current, respectively. The objective of the control scheme is to design $D(t)$ such that $V_o(t) \to V_d(t)$ as $t \to \infty$, where $V_d(t)$ is the sinusoidal output voltage trajectory defined by desired amplitude,

frequency and phase. To facilitate the control development, the following assumptions are made.

Assumption 1: L, C, R, V_{in} are known, constant system parameters.

Assumption 2: The output voltage, $V_o(t)$, is measurable.

Assumption 3: The load current is bounded, i.e. $I_o \in \mathcal{L}_\infty$.

Assumption 4: The desired voltage trajectory and its first and second time derivatives are bounded, i.e. $V_d(t), \dot{V}_d(t), \ddot{V}_d(t) \in \mathcal{L}_\infty$.

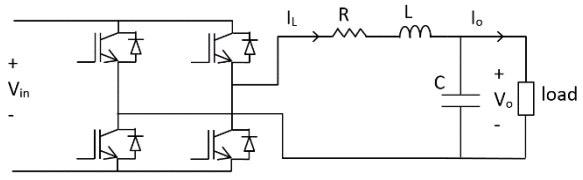

Fig. 6.1 H-Bridge inverter with output *LC* filter.

6.2 Control System Development

The designed control solution should be able to meet the previously defined control objective in the absence of inductor and output current measurements. To facilitate the controller and observers development and characterize their performance, the tracking errors signals $e(t)$, $\hat{\eta}(t)$ and observation error signals , $\tilde{I}_L$, $\tilde{I}_o$ are defined as follows:

$$e \triangleq V_d - V_o \tag{6.3}$$

$$\hat{\eta} \triangleq I_d - \hat{I}_L \tag{6.4}$$

$$\tilde{I}_L \triangleq \hat{I}_L - I_L \tag{6.5}$$

$$\tilde{I}_o = I_o - \hat{I}_o \tag{6.6}$$

where $\mathrm{I_d(t)}$ is an auxiliary control trajectory for the observed inductor current which will be defined in the proceeding controller development , $\mathrm{\hat{I}_L(t)}$ and $\mathrm{\hat{I}_o(t)}$ are the observed inductor and output current, respectively.

In a switched-mode converter some level of ripple is always present in the inductance current, $\mathrm{I_L(t)}$ as a result of switching. Due to this ripple, the measurement of inductor current is always noisy and introduces a high level of disturbance to the control system, which is typically designed based on a cycle average model. In this work an observer for $\mathrm{I_L(t)}$ denoted as $\mathrm{\hat{I}_L(t)}$ is developed to replace the measured inductor current in the subsequent closed loop controller development.

Taking the derivative of both sides of (6.5) and utilizing (6.1) gives the following:

$$L\dot{\tilde{I}}_L = L\dot{\hat{I}}_L - V_{in}D + RI_L + V_o. \tag{6.7}$$

The subsequent stability analysis and structure of (6.7) motivate the design of the inductor current observer as follows

$$\dot{\hat{I}}_L \triangleq \frac{1}{L}\left[V_{in}D - R\hat{I}_L - V_o - \frac{K_1 L}{C}\hat{\eta} - e\right] \tag{6.8}$$

where $\mathrm{K_1}$is a positive control gain. Substituting $\mathrm{\dot{\hat{I}}_L}$ from (6.8) into (6.7) results in the following equation for the observer error system.

$$L\dot{\tilde{I}}_L \triangleq -R\tilde{I}_L - \frac{K_1 L}{C}\hat{\eta} - e. \tag{6.9}$$

Substituting the system dynamics equations from (6.1) and (6.2) into the time derivative of (6.3) and (6.4) the following equations can be obtained for the open loop error system where (6.4), (6.5) and (6.8) are also utilized:

$$C\dot{e} = C\dot{V}_d - I_d + \hat{\eta} + \tilde{I}_L + I_o \tag{6.10}$$

$$L\dot{\hat{\eta}} = L\dot{I}_d - V_{in}D + R\hat{I}_L + V_o + \frac{K_1 L}{C}\hat{\eta} + e. \tag{6.11}$$

The mathematical form of (6.10) and subsequently presented stability analysis motivates the following inductor current trajectory:

$$I_d = C\dot{V}_d + K_1 e + I_o. \tag{6.12}$$

Examining the form of (6.11) we see that reduction of the error equation to a desirable closed loop form requires compensation of the term $\dot{I}_d(t)$. Taking the time derivative of (6.12), we will see that $\dot{I}_d(t)$ includes the term $\dot{I}_o(t)$. While a numerical derivative of the output current $\dot{I}_o(t)$ is possible to calculate, taking the derivative of a noisy current measurement is not a practical solution. An alternative method is to replace this measurement and numerical derivative with an output current observer which includes a derivative update law. In a PWM-VSI the switching and sampling frequency are typically orders of magnitude higher than the fundamental frequency. Therefore, in comparison with the sampling and switching frequencies, the current is changing very slowly, so that it can be approximated as a constant [66]. With this assumption from (6.6) we have:

$$\dot{\tilde{I}}_o = -\dot{\hat{I}}_o(t). \tag{6.13}$$

Substituting for $I_o(t)$ from (6.6), we can rewrite (6.10) and modify (6.12) as:

$$C\dot{e} = C\dot{V}_d - I_d + \hat{\eta} + \tilde{I}_L + \hat{I}_o + \tilde{I}_o \tag{6.14}$$

$$I_d \triangleq C\dot{V}_d + K_1 e + \hat{I}_o. \tag{6.15}$$

Motivated by the subsequent stability analysis the duty ratio control signal, $\mathrm{D(t)}$, is defined as :

$$D = \frac{1}{V_{in}}\left[w + 2e + (K_2 + \frac{K_1 L}{C})\hat{\eta}\right] \tag{6.16}$$

where $sgn(.)$ is the signum function, K_2 is a positive control gains, and

$$w \triangleq LC\ddot{V}_d + LK_1\dot{V}_d - \frac{K_1 L}{C}\hat{I}_L + R\hat{I}_L + V_o + L\,\dot{\hat{I}}_o. \tag{6.17}$$

Substituting (6.15)-(6.17) into the open loop error systems defined in (6.11) and (6.14) results in the following closed loop error system equations

$$C\dot{e} = -K_1 e + \hat{\eta} + \tilde{I}_L + \tilde{I}_o \tag{6.18}$$

$$L\dot{\hat{\eta}} = \frac{K_1 L}{C}\tilde{I}_L + \frac{K_1 L}{C}\tilde{I}_o - K_2\hat{\eta} - e. \tag{6.19}$$

The form of (6.18) and (6.19) and the subsequent stability analysis motivate the following update law for the output current observer

$$\dot{\hat{I}}_o \triangleq K_3(e + \frac{LK_1}{C}\hat{\eta}) \tag{6.20}$$

where K_3 is a positive control gain.

6.2.1 Stability Analysis

Theorem 1: Using the closed loop error system equations found in (6.18), (6.19) and the observer error equation found in (6.9), the error signals defined in (6.3)-(6.5) are regulated as

$$e(t), \hat{\eta}(t), \tilde{I}_L(t) \to 0 \ \ as \ \ t \to \infty.$$

Proof: A non-negative scalar function $S(t)$ is defined in (6.21).

$$S \triangleq \frac{1}{2}Ce^2 + \frac{1}{2}L\hat{\eta}^2 + \frac{1}{2}L\tilde{I}_L^2 + \frac{1}{2}K_3^{-1}\tilde{I}_o^2 \tag{6.21}$$

Taking the derivative of (6.21) with respect to time and substituting the error signals from (6.9), (6.13), (6.18) and (6.19), after some mathematical simplifications, the expression in (6.22) is obtained where (6.20) is also utilized.

$$\dot{S} = -K_1 e^2 - K_2\hat{\eta}^2 - R\tilde{I}_L^2 \tag{6.22}$$

From (6.21) and (6.22) it is clear that $e(t), \hat{\eta}(t), \tilde{I}_L(t) \in \mathcal{L}_2 \cap \mathcal{L}_\infty$ and $\tilde{I}_o \in \mathcal{L}_\infty$. From (6.3) and the fact that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_o(t) \in \mathcal{L}_\infty$. From (6.6) along with Assumption 3 we can see that $\hat{I}_o \in \mathcal{L}_\infty$. From (6.15) along with Assumption 4 it is clear that $I_d(t) \in \mathcal{L}_\infty$. From (6.4) and (6.5) we can see that $\hat{I}_L(t), I_L(\mathrm{t}) \in \mathcal{L}_\infty$. From (6.20) it is clear that $\dot{\hat{I}}_o(t) \in \mathcal{L}_\infty$. Now from (6.16) and (6.17) we can see that all the signals contributed in the definition of $D(t)$ are bounded, therefore $D(t) \in \mathcal{L}_\infty$. From (6.9), (6.18) and (6.19) along with the previously stated bounding statements it is clear that $\dot{\tilde{I}}_L(\mathrm{t}), \dot{e}(t), \dot{\hat{\eta}}(\mathrm{t}) \in \mathcal{L}_\infty$, respectively. Hence it is clear that all signals in the closed loop are bounded. Since $e(t), \hat{\eta}(t), \tilde{I}_L(\mathrm{t}) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t), \dot{\hat{\eta}}(t), \dot{\tilde{I}}_L(t) \in \mathcal{L}_\infty$, Barbalat's Lemma [49] can be utilized to prove that $e(t), \hat{\eta}(t), \tilde{I}_L(\mathrm{t}) \to 0 \ \ as \ t \to \infty$. Thus completing the proof of the theorem.

6.3 Simulation Result

To validate the effectiveness of the proposed observers and control design a numerical simulation was performed. The PLECS toolbox is used with Matlab/Simulink to model the instantaneous circuit dynamics of the inverter and the control schemes. The parameters used for the inverter circuit and the control scheme are summarized in Table 6.1.

Table 6.1 System Parameters

System Parameters	Value	System Parameters	Value
Output AC voltage	120 Vrms	Load1active pawer, P_1	2 kW
AC voltage frequency, f	60 Hz	Load1 reactive pawer, Q_1	1 kVar
Supply DC voltage, V_{in}	360 V	Load2 active pawer, P_2	1 kW
Filter inductance, L	10 mH	Load2 crest factor	2.5
Inductor Resistance, R	0.1 Ω	Backstepping gain, K_1	10
Filter capacitance, C	50 µF	Backstepping gain, K_2	50
Switching Frequency, f_{sw}	10 KHz	Load-current observer gain, K_3	0.5

In the first study, the transient and steady state performance of the proposed control schemes under linear resistive-inductive load, Load1, is investigated. Fig. 6.2 shows the output voltage and the output current of the inverter. Tracking errors, $e(t)$ and $\hat{\eta}(t)$, are depicted in Fig. 6.3. As can be seen in these figures excellent reference tracking is achieved with steady-state peak error less than 0.1%.

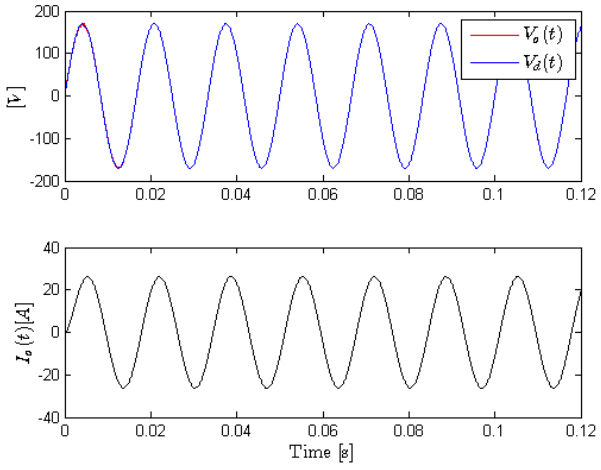

Fig. 6.2 Transient and steady-state results under linear load, Load1.

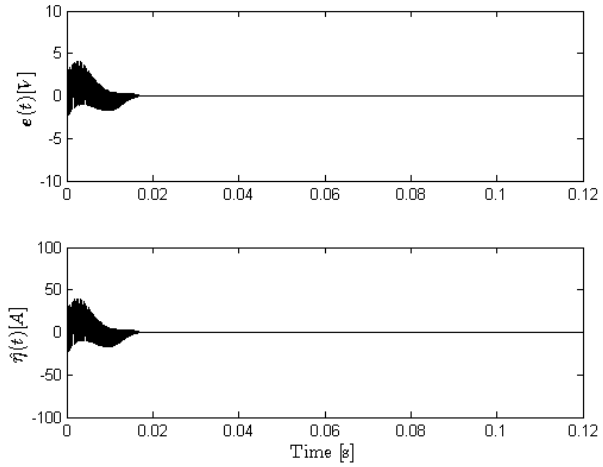

Fig. 6.3 Transient and steady-state errors under under linear load, Load1.

A second study evaluates the transient and steady state performance of the proposed control scheme under a worst case operation scenario where a highly distorting load is used. The nonlinear load, Load2, is a rectifier with output capacitor and a resistive load. The results under nonlinear rectifier load are illustrated in Fig. 6.4 and 6.5. Despite highly distorted load current, output voltage regulation is achieved with steady-state peak error less than 3%. The total harmonic distortion of the output voltage for both linear and nonlinear loads is less than 0.8 % which fulfills total voltage distortion limits of IEEE 519 (THD < 5%) and EN 50160 (THD < 8 %) for US and European power systems, respectively.

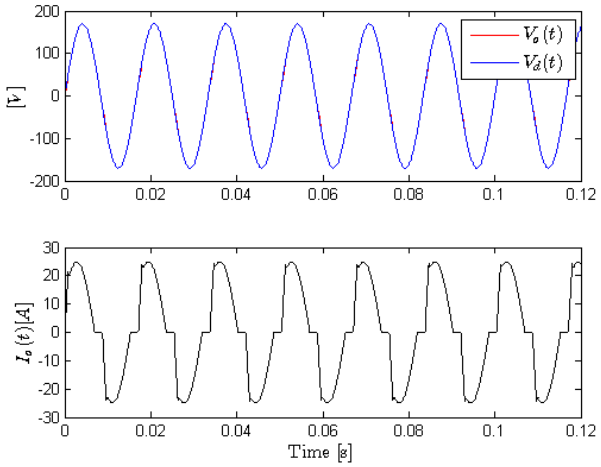

Fig. 6.4 Transient and steady-state results under nonlinear load, Load2.

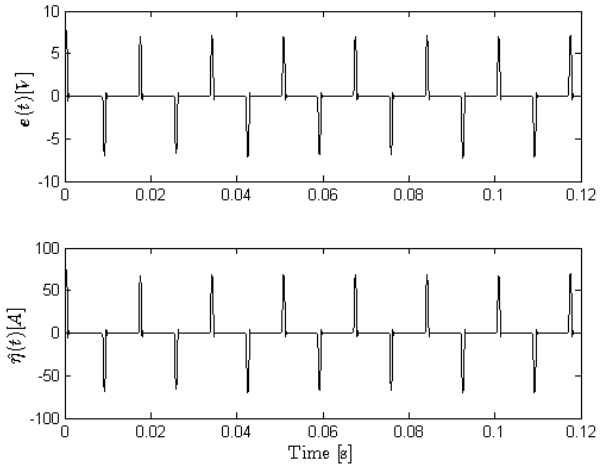

Fig. 6.5 Transient and steady-state errors under nonlinear load, Load2.

In a final study, the transient response for a load step change from no load to the nominal, 2 [kW], resistive load is considered. Due to the excellent transient performance of the proposed control scheme, as can be seen in Fig. 6.6 and 6.7, the output voltage recovers in less than 4 [ms] with very little variations in the output voltage compared to the reference during the transition.

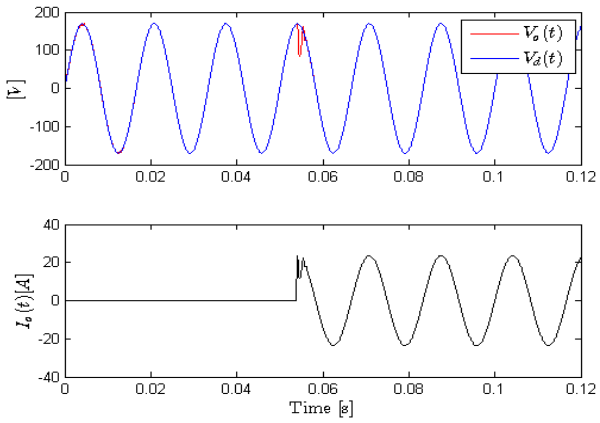

Fig. 6.6 Transient results in response to no load to nominal resitive load step change.

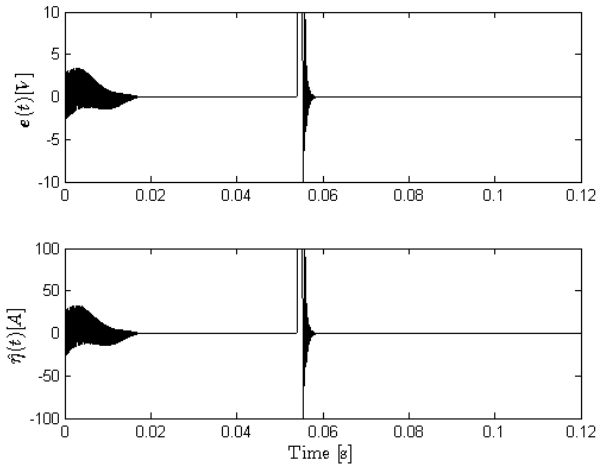

Fig. 6.7 Transient errors in response to no load to nominal resistive load step change.

6.4 Summary

A backstepping control scheme combined with an inductor current observer and a load-current observer were developed for an H-Bridge inverter with output LC filter sourcing linear and nonlinear loads. The proposed inductor current and load current observers eliminate the need for expensive and problematic current sensors. The system

performance was evaluated in terms of tracking performance, stability, system dynamics, and THD and validated via simulation. Using a simple LC output filter the output voltage THD was limited within 0.8% which fulfills IEEE 519 and EN 50160 for US and European power systems, respectively.

CHAPTER 7

FILTER-BASED CONTROL OF POWER ELECTRONICS INTERFACES

In this chapter, a filter-based control scheme is developed for buck-type converters. This approach relies only on a single output voltage measurement to reduce the system cost as well as measurement noise and disturbance injected by output current and/or inductor current measurements [67]. Although a single output voltage measurement is sufficient for the control of the power converter, to the best knowledge of the authors, the majority of the existing control approaches also require an inductor current measurement. Using two measurements gives these controllers improved system stability and dynamic performance through both output voltage and inductor current regulation. For example, a simple multiloop control technique utilizes two traditional Proportional, Integral, and Derivative (PID) controllers to regulate both output voltage and inductor current in the voltage and current control loops, respectively. In the majority of the control schemes presented for the control of power converters, at least two sensors are used to measure the output voltage and the inductor current. In practice this inductor current measurement has a significant amount of ripple and measurement noise resulting from the switching scheme. This noise and ripple are then propagated into the control algorithm adding noise and disturbance to the system. In this chapter a filter-based controller with only single output voltage

measurement is presented to eliminate the need for costly current sensors to measure the inductor and/or output currents. The elimination of the sensor along with the removal of current ripple and noise from the control algorithm provides an advantage over previous methods. The high frequency noise resulting from PWM switching is inherently filtered out of the output voltage measurement by the LC filter of the converter. Also, our model compensates for an unknown disturbance in the model. Various system uncertainty including dead-time in modulation scheme, voltage drop across switching devices and input voltage deviations are compensated with this unknown disturbance observer. A Lyapunov stability analysis proves that the sinusoidal voltage tracking objective is achieved by the controller with all signals remaining bounded. Experimental results further validate this approach.

7.1 System Model

Fig. 7.1 demonstrate a general class of PWM converters consisting of a PWM switching circuit followed by an output *LC* filter. This class of PWM covertures includes a wide variety of both dc-dc and dc-ac converters such as buck, forward, push-pull, full and half-bridge converters and inverters with output *LC* filter. All the converters/ inverters in this class can be considered as derivatives of the basic buck converter. Because of the same dynamic model for all the converter/inverter in this class, any controller developed for each is applicable for others as well. Applying the state averaging method, and PWM switching scheme the average model for a buck-type converter can be written as follows [47]:

$$L\dot{I}_L = V_{in}(D + d_o) - RI_L - V_o \tag{7.3}$$

$$C\dot{V}_o = I_L - I_o \tag{7.2}$$

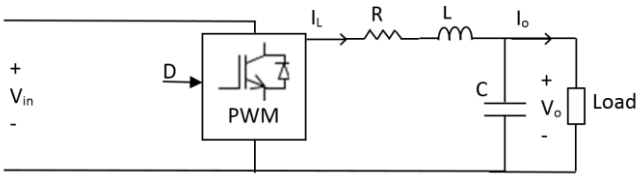

Fig. 7.1 Buck-type converter.

where L, C, R are the inductance, capacitance and series resistance of the inductance, respectively. V_{in} is the input supply voltage, $D(t)$ is the PWM duty ratio, d_o is a semi-constant unknown disturbance and $I_L(t)$ is the inductor current. $V_o(t)$, and $I_o(t)$ are the output voltage and output current, respectively. In this model, the load can be a passive load or a court source load. The objective of the control scheme is to design $D(t)$ such that $V_o(t) \to V_d(t)$ as $t \to \infty$, where $V_d(t)$ is the desired output voltage trajectory. Taking derivative of (7.2) and substituting for $\dot{I}_L(t)$ from (7.1) the following second order equation is obtained to represent the system dynamics of the buck converter.

$$m\ddot{V}_o + a\dot{V}_o + V_o = V_{in}D + u_o \tag{7.3}$$

$$u_o \triangleq V_{in}d_o - RI_o - L\dot{I}_o. \tag{7.4}$$

Where $m \triangleq LC$, $a \triangleq RC$, and the lumped disturbance u_o is defined as in (7.4).

7.2 Filter-Based Control Development

To facilitate the control development, the following assumptions are made.

Assumption 1: L, C, R, V_{in} are known, constant system parameters.

Assumption 2: The output voltage $V_o(t)$ is measurable.

Assumption 3: The load current and its first derivative and disturbance are bounded, $I_o, \dot{I}_o(t), d_o \epsilon \mathcal{L}_\infty$, and are slowly time varying in the sense that $\dot{u}_0(t) \approx 0$.

Assumption 4: The desired voltage trajectory and its first and second time derivatives are bounded, i.e. $V_d(t), \dot{V}_d(t), \ddot{V}_d(t) \in \mathcal{L}_\infty$.

To facilitate the controller development and characterize its performance, the tracking error signal $e(\mathrm{t})$ and filtered error signals, $\mathrm{r}_f(t), e_f(t)$ are defined as follows:

$$e \triangleq V_d - V_o \tag{7.5}$$

$$\dot{p} \triangleq -K_1 r_f + (K_2 + \alpha)\big(\alpha e - r_f\big) - e - e_f \tag{7.6}$$

$$r_f \triangleq p + (K_2 + \alpha)e \tag{7.7}$$

where K_1, K_2, α are positive gains, $p(t)$ is an auxiliary variable defined for filter implementation and $e_f(t)$ is defined with the following differential equation.

$$\dot{e_f} \triangleq r_f - \alpha e_f \tag{7.8}$$

To further the control development the following error signal is also defined:

$$\eta \triangleq \dot{e} + \alpha e - r_f \tag{7.9}$$

Taking derivative of (7.7) and using (7.6) and (7.9) results in:

$$\dot{r_f} = -K_1 r_f + (K_2 + \alpha)\eta - e - e_f \tag{7.10}$$

Taking derivative of (7.9) and utilizing (7.9), (7.10) and the second derivative of (7.5) after some mathematical simplifications results in:

$$\dot{\eta} = \ddot{V}_d - \ddot{V}_o + (K_1 + \alpha)r_f - K_2\eta - \alpha^2 e + e + e_f. \tag{7.11}$$

Multiplying both sides of (7.11) by m and substituting for $m\ddot{V}_o$ from (7.3), we get (7.12) after utilizing (7.5) and (7.9):

$$\begin{aligned} m\dot{\eta} = m\ddot{V}_d + m(K_1 + \alpha)r_f - mK_2\eta - m\alpha^2 e \; + m(e + e_f) + a\dot{V}_d \\ + a\alpha e \\ -ar_f - a\eta + V_o - V_{in}D - u_o \end{aligned} \tag{7.12}$$

From (7.12) and motivated by the subsequent stability analysis the duty ratio control signal is defined as:

$$\begin{aligned} D \triangleq \frac{1}{V_{in}}[m\ddot{V}_d + m(K_1 + \alpha)r_f - m\alpha^2 e + m(e + e_f) + a\dot{V}_d + a\alpha e \\ -ar_f + V_d + (K_2 + \alpha)r_f - \hat{u}_0] \end{aligned} \tag{7.13}$$

where $\hat{u}_0$ is the estimated disturbance with the following estimation error:

$$\tilde{u}_0 \triangleq u_o - \hat{u}_0. \tag{7.14}$$

Finally, the closed loop error system is obtained by substituting (7.13) in (7.12) as follows.

$$m\dot{\eta} = -mK_2\eta - a\eta - e - (K_2 + \alpha)r_f - \tilde{u}_0 \tag{7.15}$$

From Assumption 3 and (7.14) we have:

$$\dot{\hat{u}}_0 \approx -\dot{\tilde{u}}_0. \tag{7.16}$$

Motivated by the subsequent stability analysis the update law for $\hat{u}_0$is defined as:

$$\dot{\hat{u}}_0 \triangleq -K_3\eta \tag{7.17}$$

where K_3 is a positive constant gain. As can be inferred from (7.9), $\eta(t)$ is not a measurable signal. By taking the integral of (7.17) and substituting for $\eta(t)$ from (7.9) the update law for $\hat{u}_0(t)$ becomes realizable as:

$$\hat{u}_0(t) = -K_3\left[\int_0^t \left(\alpha e(\tau) - r_f(\tau)\right) d\tau + e(t) - e(0)\right]. \tag{7.18}$$

7.2.1 Stability Analysis

Theorem 1: Using the closed loop error system equation found in (7.15) the error signals defined in (7.5), (7.7), (7.8) and (7.9) are regulated as follows:

$$e(t), e_f(t), r_f(t), \eta(t) \to 0 \text{ as } t \to \infty.$$

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined in (7.19).

$$S \triangleq \frac{1}{2}e^2 + \frac{1}{2}e_f^2 + \frac{1}{2}r_f^2 + \frac{1}{2}m\eta^2 + \frac{1}{2K_3}\tilde{u}_0^2 \tag{7.19}$$

Taking the derivative of (7.19) with respect to time and substituting $\dot{e_f}(t), \dot{e}(t), \dot{r_f}(\mathrm{t})$ and $m\dot{\eta}(t)$ from (7.8), (7.9), (7.10) and (7.15), respectively, after some mathematical simplifications the expression in (7.20) is obtained where (7.16) and (7.17) are also utilized.

$$\dot{S} = -\alpha e^2 - \alpha e_f^2 - K_1 r_f^2 - K_2 m\eta^2 - a\eta^2 \tag{7.20}$$

From (7.19) and (7.20) it is clear that $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_2 \cap \mathcal{L}_\infty$ and $\tilde{u}_0 \in \mathcal{L}_\infty$. From (7.5) and the fact that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_o(t) \in \mathcal{L}_\infty$. From (7.4) and (7.14) along with Assumption 3 it is clear that $\hat{u}_0 \in \mathcal{L}_\infty$. Now From (7.13) along with $\ddot{V}_d(t), \dot{V}_d(t), V_d(t) \in \mathcal{L}_\infty$, we can see that all the signals contributed in the definition of $D(t)$ are bounded, therefore $D(t) \in \mathcal{L}_\infty$. From (7.8)-(7.10) along with the previously stated bounding statements it is clear that $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}) \in \mathcal{L}_\infty$. With $\dot{e}(t) \in \mathcal{L}_\infty$, (7.5) can be used to deduce $\dot{V}_o(t) \in \mathcal{L}_\infty$. From (7.3) it can be inferred that $\ddot{V}_o(t) \in \mathcal{L}_\infty$. Hence it is clear that all signals in the closed loop are bounded. From (7.11) it is clear that $\dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$. Since $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}), \dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$, Barbalat's

Lemma [49] can be utilized to prove that $e(t), e_f(t), r_f(t), \eta(t) \to 0 \ as \ t \to \infty$. Thus completing the proof of the theorem.

7.3 Experimental Results

7.3.1 Buck Converter

To verify the performance of the proposed controller and observers in real-time application, a prototype of closed loop buck dc-dc converter is used as shown in Fig. 7.2. The NI CompactRIO and the commercial software LabVIEW are used for implementation of the controller algorithm. The control algorithm is first developed using LabVIEW software on the personal computer and then downloaded to the onboard FPGA of the CompactRIO. The real-time experimental results were sent back to the personal computer through real time controller of CompactRIO for monitoring and data logging. Table 7.1 summarizes the system parameters used for experimental test.

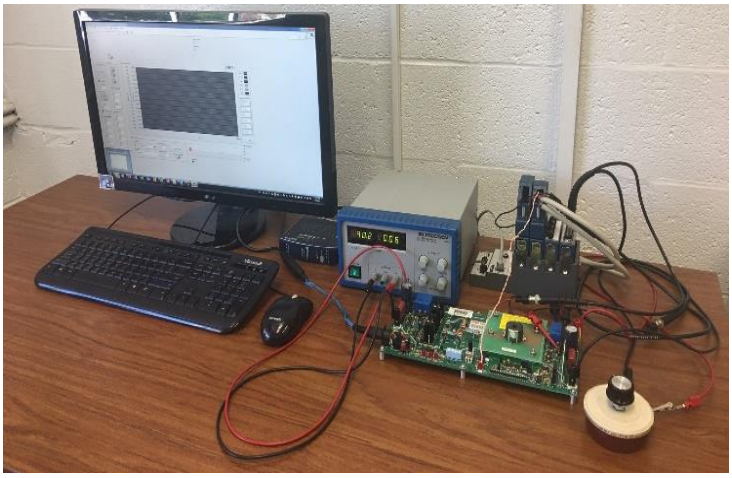

Fig. 7.2 Experimental setup of the buck converter.

Table 7.1 Buck Converter System Parameters

Parameter	Value	Units
L	104	µH
C	680	µF
R	0.1	Ω
V_{in}	40	V
Load Resistance (R_{load})	5	Ω
K_1	7	-
K_2	1	-
K_3	10	-
α	3	-
Switching Frequency (f_{sw})	10	KHz

Fig. 7.3 shows the tracking performance of the converter. This figure demonstrates both steady-state and transient response of the system in response to a step change in desired output voltage. Error signal, (t), and duty cycle, D(t), are seen in Fig. 7.4 and 7.5 respectively. From this figures, it is clear that the converter and its developed controller work well within the desired parameters in closed loop control, achieving an excellent voltage regulation. Fig.6 shows the estimated system disturbance.

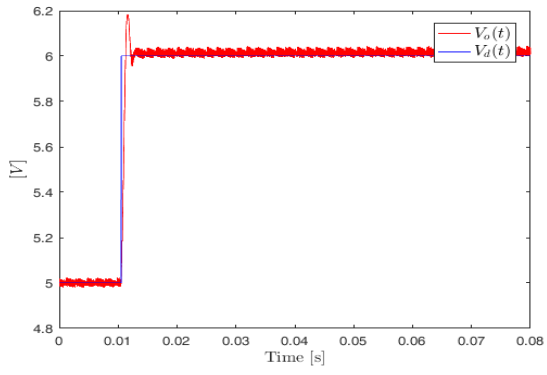

Fig. 7.3 Output voltage, $V_o(t)$, and the desired voltage, $V_d(t)$, of the buck converter.

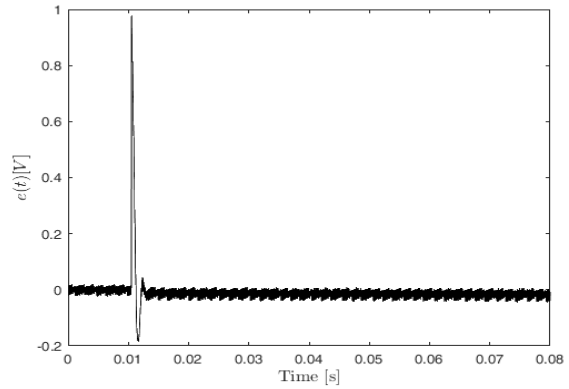

Fig. 7.4 Voltage tracking error, (t) of the buck converter.

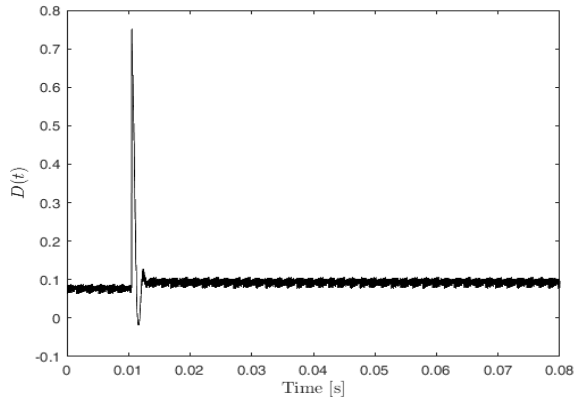

Fig. 7.5 The duty ratio control signal, D(t) of the buck converter.

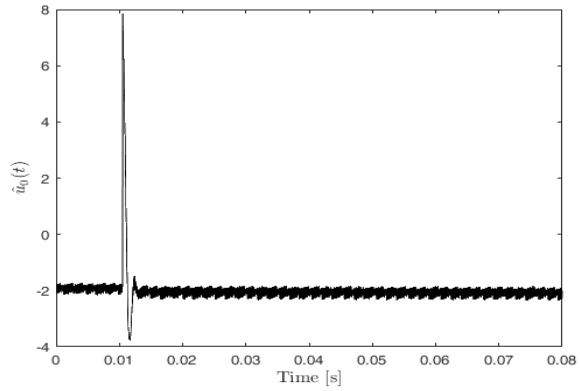

Fig. 7.6 The estimated system disturbance, $\hat{u}_0(t)$ of the buck converter.

7.3.2 H-Bridge-Inverter

The test rig used for investigating the performance of the proposed controller and observers is shown in Fig. 7.7 for an H-bridge inverter. Again, in this setup the NI CompactRIO and the commercial software LabVIEW are used for implementation of the controller algorithm. The control algorithm requires only one voltage sensor to measure the output voltage, $V_o(t)$. For the purposes of data logging and visualization a current sensor is also utilized for the output current measurement. Table 7.2 summarizes the system parameters used for experimental test. The steady state performance of the proposed control scheme under linear resistive-inductive load is shown in Fig.7. This figure shows the desired, $V_d(t)$, and actual output voltage, tracking error, $e(t)$, and the output current as well as the control signal, $D(t)$, for the H-Bridge inverter. As can be seen in this figures, the excellent reference tracking with the steady-state peak error less than 0.7% is achieved for the proposed control scheme.

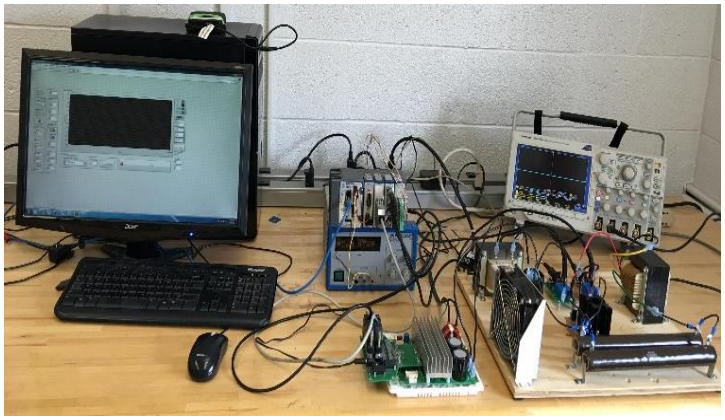

Fig. 7.7 Experimental setup of the H-Bridge inverter.

Table 7.2 System Parameters

	Parameter	Value	Units
Inverter	L	10	mH
	C	100	µF
	R	0.1	Ω
	V_o (peak-to-peak)	200	V
	V_{in}	350	V
	f	60	Hz
	Switching Frequency (f_{sw})	5	KHz
Nonlinear Load .Resistor-Inductor Load	L_{load1}	32	mH
	R_{load1}	37.5	Ω
	C_{load2}	220	µF
	R_{load2}	250	Ω
Controller Gain	K_1	20	-
	K_2	4	-
	K_3	1	-
	α	2.5	-

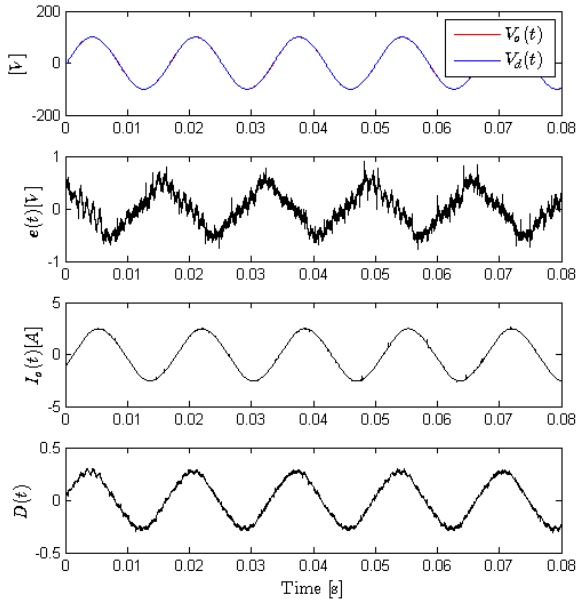

Fig. 7.7 Steady-state results under *RL* load for the H-bridge inverter.

In Fig. 7.9, the performance of the proposed control scheme is evaluated under a worst-case operation scenario where a highly distorting load is used consisting of a full wave rectifier bridge feeding a 250 [Ω] resistor in parallel with a 220 [μF] capacitor. Despite highly distorted load current, the output voltage regulation with the steady-state peak error less than 1% is achieved for the H-bridge inverter.

The transient response to a -50% step change in amplitude of reference voltage, $V_d(t)$, under nominal 37.5 [Ω] resistive load is demonstrated in Fig. 7.10. As it can be seen in this figure, to represent the worst case operation, the reference command is changed when the output voltage is at its peak value. Due to the excellent transient performance of the proposed control scheme, the output voltage recovers in less than half of a cycle.

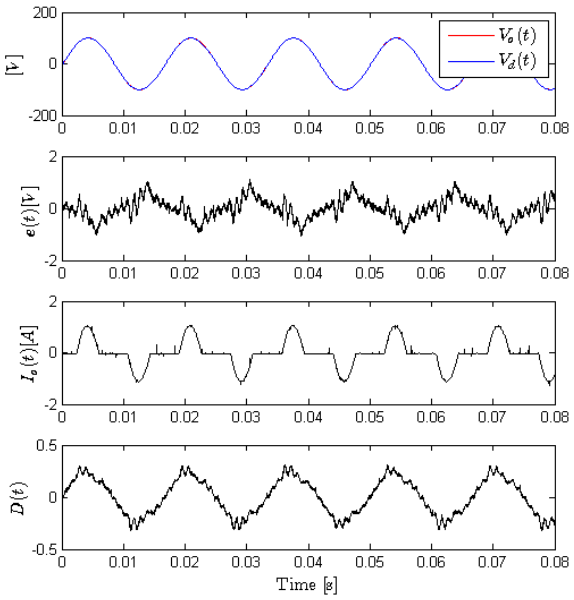

Fig. 7.7 Steady-state results under highly distorting nonlinear load for the H-bridge inverter.

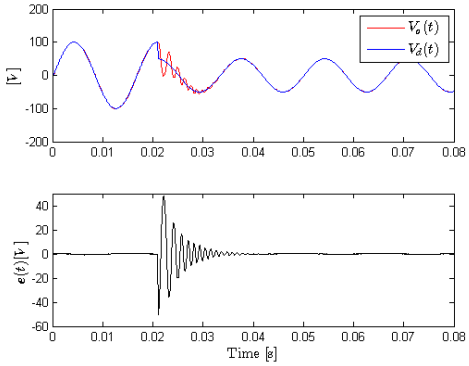

Fig. 7.7 Transient results in response to -50% step change in amplitude of the reference voltage under resistive load for the H-bridge onverter.

7.4 Summary

In this chapter a filter-based control scheme relying on only a single output voltage measurement is proposed to regulate the output voltage of a buck-type converter. The performance of the control scheme is confirmed through experimental results in terms of steady-state tracking error, stability as well as transient response. In addition to the lower cost resulting from removing current measurement sensors, the effectiveness of this scheme is demonstrated in terms of excellent voltage tracking, good transient response and insensitivity to the load variation.

CHAPTER 8

FILTER-BASED CONTROLLER WITH UNKNOWN SYSTEM PARAMETERS

This chapter presents a filter-based control scheme for an H-Bridge inverter with output LC filter [68]. This approach relies only on a single output voltage measurement to reduce the system cost as well as measurement noise and disturbance injected by output current and/or inductor current measurements. To reduce the controller sensitivity to the system parameters, the proposed controller is developed for unknown system parameters. As it was mentioned in the Introduction section, due to the same system dynamics, this controller scheme is applicable for any converter/inverter in the class of buck-type converters.

In the majority of the control schemes presented for the control of VSI with output LC filter, at least two sensors are used to measure the output voltage and the inductor current. In practice this inductor current measurement has a significant amount of ripple and measurement noise resulting from the switching scheme. This noise and ripple are then propagated into the control algorithm adding noise and disturbance to the system. Some control schemes use capacitor current measurement instead of the inductor current measurement [14], [39], [40], [41] where the same problem remains. Also some works use an output current sensor in addition to the other two sensors [14], [26], [57], [39] to reduce

the effect of the high frequency noise and ripple resulting from switching, utilization of a low-pass filter (LPF) is suggested. Addition of LPF introduces phase delays, which can have an adverse effect on the control schemes, which can limit any performance improvement.

In [69] and [70] a filter-based discontinuous tracking controller for a general class of nonlinear, multi-input/multi-output (MIMO) mechanical systems with no disturbances is presented. In the present work a modified filter-based control scheme is proposed which utilizes the known system structure of a second order linear system and compensates for unknown disturbances. This scheme removes the need for parameter knowledge by utilizing a robust algorithm comprising a nonlinear sliding term which compensates for parameter uncertainties.

In this chapter a filter-based controller with only single output voltage measurement is presented to eliminate the need for costly current sensors to measure the inductor and/or output currents. The elimination of the sensor along with the removal of current ripple and noise from the control algorithm provides an advantage over previous methods. The high frequency noise resulting from PWM switching is inherently filtered out of the output voltage measurement by the LC filter of the inverter. Also, to reduce the control sensitivity to the system parameters and compensate for parameter variation, the control scheme is developed for unknown system parameters. A Lyapunov stability analysis proves that the sinusoidal voltage tracking objective is achieved by the controller with all signals remaining bounded. Experimental results further validate this approach.

8.1 System Model

An H-Bridge inverter with an output *LC* filter as seen in Fig. 8.1 is used for DC to AC power conversion. Applying the state averaging method and unipolar PWM switching scheme, the average model for an H-Bridge inverter can be written as follows [47]:

$$L\dot{I}_L = V_{in}(D + d_o) - RI_L - V_o \tag{8.1}$$

$$C\dot{V}_o = I_L - I_o \tag{8.2}$$

where L, C, R are the inductance, capacitance and series resistance of the inductance, respectively. V_{in} is the input supply voltage, $D(t)$ is the PWM duty ratio, d_o is a constant unknown disturbance and $I_L(t)$ is the inductor current. $V_o(t)$, and $I_o(t)$ are the output voltage and output current, respectively. The objective of the control scheme is to design $D(t)$ such that $V_o(t) \to V_d(t)$ as $t \to \infty$, where $V_d(t)$ is the desired sinusoidal output voltage trajectory defined by amplitude, frequency and phase. Taking derivative of (8.2) and substituting for $\dot{I}_L(t)$ from (8.1) the following second order equation is obtained to represent the system dynamics of the inverter.

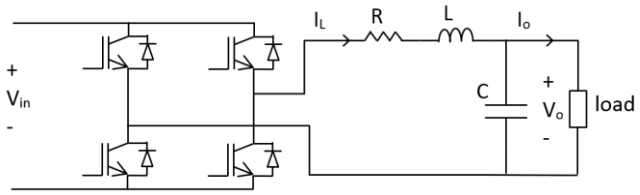

Fig8.1 H-Bridge inverter with output *LC* filter.

$$m\ddot{V}_o + a\dot{V}_o + V_o = V_{in}D + u_o \tag{8.3}$$

Where $m \triangleq LC$, $a \triangleq RC$, and the lumped disturbance u_o is defined as follows:

$$u_o \triangleq V_{in} d_o - R I_o - L \dot{I}_o. \tag{8.4}$$

8.2 Filter-Based Control for Unknown System Parameters

For the control development, a general case in which the inverter parameters including L, C, R are unknown is considered. This is a practical approach as parameter values change over the life of operation. Also parameter tolerance can be a performance issue. To facilitate the control development, the following set of assumptions are made.

Assumption 1: L, C, R, are unknown and time varying, but limited in a specific range such that:

$$\underline{m} < m(t) < \overline{m} \tag{8.5}$$

$$\underline{a} < a(t) < \overline{a} \tag{8.6}$$

Assumption 2: The rate of change of m with time is limited such that:

$$\dot{m}(t) < \overline{M}. \tag{8.7}$$

Assumption 3: The output voltage $V_o(t)$ is measurable.

Assumption 4: The input voltage V_{in} is known and constant.

Assumption 5: The load current and disturbance have the following properties: $I_o, \dot{I}_o(t), d_o \epsilon \mathcal{L}_\infty$.

Assumption 6: $V_d(t), \dot{V}_d(t), \ddot{V}_d(t), \dddot{V}_d(\mathrm{t}) \in \mathcal{L}_\infty$.

To facilitate the controller development and characterize its performance, the tracking error signal $e(\mathrm{t})$ and filtered error signals, $r_f(t), e_f(t)$ are defined as follows:

$$e \triangleq V_d - V_o \tag{8.8}$$

$$\dot{p} \triangleq -K_1 r_f + (K_2 + \alpha)\big(\alpha e - r_f\big) - e - e_f \tag{8.9}$$

$$r_f \triangleq p + (K_2 + \alpha)e \tag{8.10}$$

where K_1, K_2, α are positive gains, $p(t)$ is an auxiliary variable defined for filter implementation and $e_f(t)$ is defined with the following differential equation.

$$\dot{e_f} \triangleq r_f - \alpha e_f \tag{8.11}$$

To further the control development the following error signal is also defined:

$$\eta \triangleq \dot{e} + \alpha e - r_f \tag{8.12}$$

Taking derivative of (8.10) and using (8.9) and (8.12) results in:

$$\dot{r_f} = -K_1 r_f + (K_2 + \alpha)\eta - e - e_f \tag{8.13}$$

Taking derivative of (8.12) and utilizing (8.12), (8.13) and the second derivative of (8.8) after some mathematical simplifications results in:

$$\dot{\eta} = \ddot{V}_d - \ddot{V}_o + (K_1 + \alpha)r_f - K_2\eta - \alpha^2 e + e + e_f. \tag{8.14}$$

Multiplying both sides of (8.14) by m and substituting for $m\ddot{V}_o$ from (8.3), we get (8.15) after utilizing (8.8) and (8.12):

$$\begin{aligned} m\dot{\eta} = m\ddot{V}_d + m(K_1 + \alpha)r_f - mK_2\eta - m\alpha^2 e + m(e + e_f) + a\dot{V}_d + a\alpha e \\ - ar_f - a\eta + V_o - V_{in}D - u_o \end{aligned} \tag{8.15}$$

From (8.15) and motivated by the subsequent stability analysis the duty ratio control signal is defined as:

$$D \triangleq \frac{1}{V_{in}}[V_d + (K_2 + \alpha)r_f - \hat{u}_0 + K_3 sgn(e - e_f)] \tag{8.16}$$

where K_3 is a positive constant gain, $sgn(.)$ is the standard signum function and $\hat{u}_0$ is the estimated disturbance with the following estimation error:

$$\tilde{u}_0 \triangleq u_o - \hat{u}_0. \tag{8.17}$$

Finally, the closed loop error system is obtained by substituting (8.16) in (8.15) as follows.

$$\begin{aligned} m\dot{\eta} = N_d + \tilde{N} - mK_2\eta - a\eta - \frac{1}{2}\dot{m}\eta - \tilde{u}_0 - e - (K_2 + \alpha)r_f \\ - K_3 sgn(e - e_f) \end{aligned} \tag{8.18}$$

with $N_d \triangleq m\ddot{V}_d + a\dot{V}_d$ and $\tilde{N}$ defined as:

$$\tilde{N} = m(K_1 + \alpha)r_f - m\alpha^2 e + m(e + e_f) + a\alpha e - ar_f + \frac{1}{2}\dot{m}\eta \tag{8.19}$$

where $\frac{1}{2}\dot{m}\eta$ is added to and subtracted from the right hand side of (8.19) and (8.18), respectively.

As the load is unknown and the load current is not measured we cannot directly account for the corresponding terms in u_o. However, we can make some simplifying assumptions to develop an appropriate observer based on the control implementation. In a PWM-VSI the switching and sampling frequency are typically orders of magnitude higher than the fundamental frequency. Therefore, in comparison with the sampling and switching frequencies, the output current and its derivative are changing very slowly, so that it can be approximated as a constant [66]. Using this fact, u_o can be approximated as:

$$\dot{\hat{u}}_0 \approx -\dot{\tilde{u}}_0. \tag{8.20}$$

Motivated by the subsequent stability analysis the update law for $\hat{u}_0$is defined as:

$$\dot{\hat{u}}_0 \triangleq -K_4\eta \tag{8.21}$$

where K_4 is a positive constant gain. As can be inferred from (8.12), η is not a measurable signal. But by taking the integral of (8.21) and substituting for η from (8.12) the update law for $\hat{u}_0$ becomes realizable as:

$$\hat{u}_0(t) = -K_4\left[\int_0^t \left(\alpha e(\tau) - r_f(\tau)\right)d\tau + e(t) - e(0)\right] \tag{8.22}$$

8.2.1 Stability Analysis

Before stating the main theorem, the following lemma is presented to be invoked later.

Lemma 1: Let the auxiliary function $L(t)$ be defined as follows:

$$L(t) \triangleq \eta(N_d - K_3 sgn(e - e_f)) \tag{8.23}$$

If K_3 is selected to meet the following gain condition:

$$K_3 > (|N_d| + \frac{1}{\alpha}|\dot{N}_d|) \tag{8.24}$$

then

$$\int_0^t L(\tau)d\tau \leq \zeta \tag{8.25}$$

where the positive constant ζ is defined as:

$$\zeta \triangleq |e(0)N_d(0)| + K_3|e(0)|. \tag{8.26}$$

Proof: See Appendix A of [70].

Theorem 2: Using the closed loop error system equation found in (8.18) the error signals defined in (8.8), (8.10), (8.11) and (8.12) are regulated as follows:

$$e(t), e_f(t), r_f(t), \eta(t) \to 0 \text{ as } t \to \infty.$$

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined as

$$S \triangleq \frac{1}{2}e^2 + \frac{1}{2}e_f^2 + \frac{1}{2}r_f^2 + \frac{1}{2}m\eta^2 + \frac{1}{2K_4}\tilde{u}_0^2 + \zeta - \int_0^t L(\tau)d\tau \tag{8.27}$$

Taking the derivative of (8.27) with respect to time and substituting $\dot{e_f}(t), \dot{e}(t), \dot{r_f}(\mathrm{t})$ and $m\dot{\eta}(t)$ from (8.11), (8.12), (8.13) and (8.18), respectively, after some mathematical simplifications the expression in (8.28) is obtained where (8.20), (8.21) and (8.23) are also utilized.

$$\dot{S} = -\alpha e^2 - \alpha e_f^2 - K_1 r_f^2 - K_2 m\eta^2 - a\eta^2 + \widetilde{N}\eta \tag{8.28}$$

To proceed we first need to find an upper bound for $|\widetilde{N}|$

$$\begin{aligned} |\widetilde{N}| &\leq [\bar{m}(K_1 + \alpha) + \bar{a}]|r_f| + \bar{m}|e_f| + [\bar{m}\alpha^2 + \bar{m} + \bar{a}\alpha]|e| + \frac{1}{2}\overline{M}|\eta| \\ &= b_1|r_f| + b_2|e_f| + b_3|e| + b_4|\eta| \end{aligned} \tag{8.29}$$

where $b_1 \triangleq [\bar{m}(K_1 + \alpha) + \bar{a}]$, $b_2 \triangleq \bar{m}$, $b_3 \triangleq [\bar{m}\alpha^2 + \bar{m} + \bar{a}\alpha]$ and $b_4 \triangleq \frac{1}{2}\overline{M}$. Assuming $K_2 = \frac{1}{\underline{m}}(K_{21} + K_{22} + K_{23} + K_{24})$where K_{21}, K_{22}, K_{23}, K_{24} are all positive and using (8.29), $\dot{S}(t)$ can be upper bounded as:

$$\begin{aligned} \dot{S} \leq\ & -\alpha e^2 - \alpha e_f^2 - K_1 r_f^2 - a\eta^2 + \left[b_1|\eta||r_f| - K_{21}\eta^2\right] + \left[b_2|\eta||e_f| - K_{22}\eta^2\right] \\ & + [b_3|\eta||e| - K_{23}\eta^2] + (b_4 - K_{24})\eta^2. \end{aligned} \tag{8.30}$$

The three bracketed terms in (8.30), each represents nonlinear damping pairs that can be upper bounded as (8.31)-(8.33) [71].

$$b_1|\eta|\left|r_f\right| - K_{21}\eta^2 \leq \frac{b_1^2 {r_f}^2}{K_{21}} \tag{8.31}$$

$$b_2|\eta|\left|e_f\right| - K_{22}\eta^2 \leq \frac{b_2^2 {e_f}^2}{K_{22}} \tag{8.32}$$

$$b_3|\eta||e| - K_{23}\eta^2 \leq \frac{b_3^2 e^2}{K_{23}} \tag{8.33}$$

Assuming the gain conditions (8.34)-(8.37) are meet, $\dot{S}(t)$ can be upper bounded as (8.38).

$$K_{21} > \frac{b_1^2}{K_1} \tag{8.34}$$

$$K_{22} > \frac{b_2^2}{\alpha} \tag{8.35}$$

$$K_{23} > \frac{b_3^2}{\alpha} \tag{8.36}$$

$$K_{24} > b_4 \tag{8.37}$$

$$\dot{S} \leq -\beta_1 r_f^2 - \beta_2 e_f^2 - \beta_3 e^2 - \beta_4 \eta^2 - a\eta^2 \tag{8.38}$$

Where $\beta_1 \triangleq K_1 - \frac{b_1^2}{K_{21}}$, $\beta_2 \triangleq \alpha - \frac{b_2^2}{K_{22}}$, $\beta_3 \triangleq \alpha - \frac{b_3^2}{K_{23}}$ and $\beta_4 \triangleq K_{24} - b_4$ are positive constants.

From (8.27) and (8.38) it is clear that $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_2 \cap \mathcal{L}_\infty$ and $\tilde{u}_0 \in \mathcal{L}_\infty$. From (8.8) and the fact that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_o(t) \in \mathcal{L}_\infty$. From (8.4) and (8.17) along with Assumption 5 it is clear that $\hat{u}_0 \in \mathcal{L}_\infty$. Now from (8.16) along with $V_d(t) \in \mathcal{L}_\infty$, we can see that all the signals contributed in the definition of $D(t)$ are bounded, therefore $D(t) \in \mathcal{L}_\infty$. From (8.11)-(8.13) along with the previously stated bounding statements it is clear that $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}) \in \mathcal{L}_\infty$. With $\dot{e}(t) \in \mathcal{L}_\infty$, (8.8) can be used to deduce $\dot{V}_o(t) \in \mathcal{L}_\infty$. From (8.3) it can be inferred that $\ddot{V}_o(t) \in \mathcal{L}_\infty$. Hence it is clear that all signals in the closed loop are bounded. From (8.14) it is clear that $\dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$. Since $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}), \dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$, Barbalat's Lemma

[49] can be utilized to prove that $e(t), e_f(t), r_f(t), \eta(t) \to 0$ $as\ t \to \infty$. Thus completing the proof of the theorem.

8.3 Experimental Results

The test rig used for verifying the performance of the proposed controller and observers is shown in Fig. 7.7. The NI CompactRIO, cRIO-9022, with cRIO-9113 chassis and the commercial software LabVIEW are used for implementation of the controller algorithm. The control algorithm is first developed using LabVIEW software on a personal computer and then downloaded to the onboard Virtex-5 LX50 FPGA of the cRIO-9113. The real-time experimental results were sent back to the personal computer through real time controller cRIO-9022 for monitoring and data logging. The dc link is fed by a single phase voltage doubler rectifier. Fig 8.2 shows a block diagram of the experimental set up. The control algorithm requires only one voltage sensor to measure the output voltage, $V_o(t)$. For the purposes of data logging and visualization a current sensor is also utilized for the output current measurement. Table 8.1 summarizes the system parameters used for experimental test.

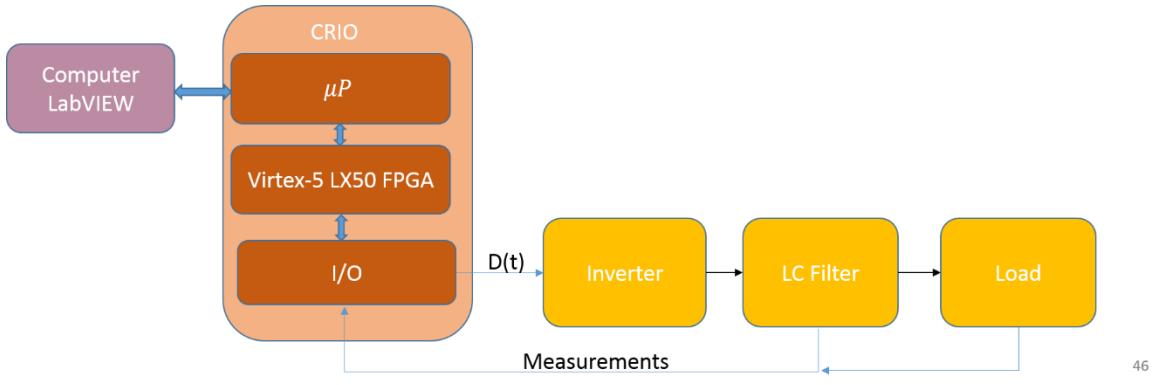

Fig. 8.2 Experimental setup block diagram.

Table 8.1 System Parameters

	Parameter	Value	Units
Inverter	L	10	mH
	C	100	μF
	R	0.1	Ω
	V_o (peak-to-peak)	200	V
	V_{in}	350	V
	f	60	Hz
	Switching Frequency (f_{sw})	5	KHz
Nonlinear Load	Resistor-Inductor Load	L_{load1}	32	mH
		R_{load1}	37.5	Ω
	C_{load2}	220	μF
	R_{load2}	250	Ω
Controller Gain	K_1	20	-
	K_2	0.5	-
	K_3	100	-
	K_4	15	-
	α	0.5	-

In the first study, the steady state performance of the proposed control scheme under linear resistive-inductive load is investigated. Fig. 8.3 shows the desired, $V_d(t)$, and actual output voltage, $V_o(t)$, the tracking error, $e(t)$, and the output current as well as the control signal, $D(t)$. As can be seen in this figure, the excellent reference tracking with the steady-state peak error less than 1.45%, is achieved for the proposed control scheme.

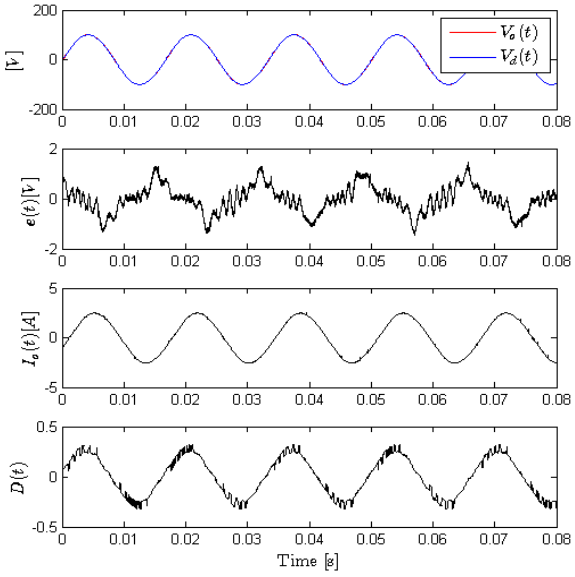

Fig. 8.3 Steady-state results under RL load.

A second study evaluates the performance of the proposed control scheme under a worst case operation scenario where a highly distorting load is used consisting of a full wave rectifier bridge feeding a 250 [Ω] resistor in parallel with a 220 [μF] capacitor. The results under nonlinear rectifier load are illustrated in Fig. 8.4. Despite highly distorted load current, the output voltage regulation with the steady-state peak error less than 2.15%, is achieved for the proposed control scheme.

A third study evaluated performance under no load operation of the inverter. Table 8.2 summarizes the results in terms of total harmonic distortion (THD) and steady-state error between the output voltage and its reference for different test cases. As it can be seen in this table voltage THD is limited within 0.76% which fulfills IEEE 519 and EN 50160 standards for US and European power systems, respectively.

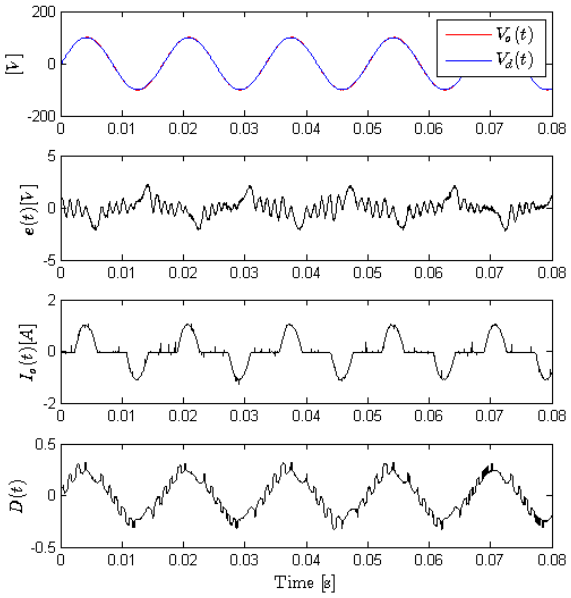

Fig. 8.4 Steady-state results under highly distorting nonlinear load.

Table 8.2 Performance Comparison

Load Type	Peak Error (%)	THD (%)
No load	1.44	0.38
RL load	1.45	0.38
Highly nonlinear load	2.15	0.76

In a final study, the transient response to a -50% step change in amplitude of reference voltage, $V_d(t)$, under nominal 37.5 [Ω] resistive load is considered. As it can be seen in Fig. 8.5, to represent the worst case operation, the reference command is changed when the output voltage is at its peak value. Due to the excellent transient performance of the proposed control schemes, the output voltage recovers in less than half of a cycle.

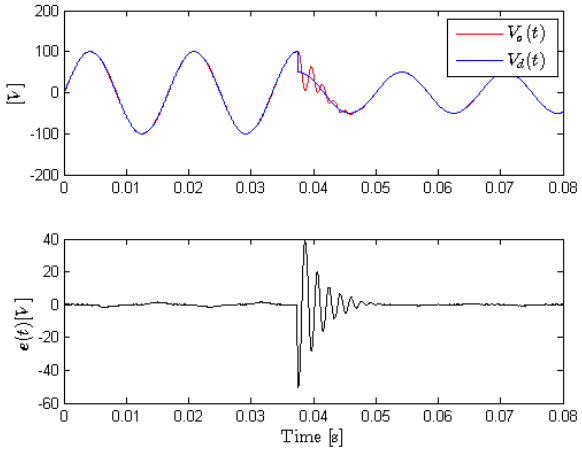

Fig. 8.5 Transient results in response to -50% step change in amplitute of the reference voltage under resistive load.

8.4 Summary

In this chapter a filter-based control scheme relying on only a single output voltage measurement is proposed to regulate the instantaneous voltage of single-phase inverter in stand-alone mode. The performance of the control scheme is confirmed through experimental results in terms of steady-state tracking error, THD, stability as well as transient response. In addition to the lower cost resulting from removing current measurement sensors, the proposed control scheme has demonstrated its effectiveness in terms of low THD, excellent voltage regulation and insensitivity to load variation, even under a nonlinear load. The development of the control scheme for unknown system parameters makes it more attractive for its robustness against parameter variations in practical systems as the system parameters are subject to change during long term operation of the system.

CHAPTER 9

FILTER-BASED CONTROLLER WITH PARAMETERS DISCREPANCY

This chapter presents a filter-based control scheme for an H-Bridge inverter with output LC filter. This approach relies only on a single output voltage measurement to reduce the system cost as well as measurement noise and disturbance injected by output current and/or inductor current measurements. Also, the proposed control algorithm is robust against parameter discrepancy. A Lyapunov stability analysis is utilized to demonstrate the control object is met and that all signals in the closed loop system are stable. Experimental results demonstrate excellent voltage tracking, insensitivity to the load and system parameter variations, and low output voltage distortion as well as the stability of the system under both linear and nonlinear loads. Since the proposed controller requires only a single output voltage measurement, this scheme eliminates the need for costly current sensors to measure the inductor and/or output currents. The elimination of the sensor along with the removal of current ripple and noise from the control algorithm provides an advantage over previous methods. The high frequency noise resulting from PWM switching is inherently filtered out of the output voltage measurement by the LC filter of the inverter. Also, the proposed control algorithm is robust against parameter discrepancy which in turn reduces the control sensitivity to the system parameters andcompensates for parameter variation. Unlike the work presented in the previous chapter

[72] which is developed for unknown system parameters, this work utilizes the nominalvalues of the system parameters and compensate for parameter discrepancies which results in a significant improvement in the system performance. A Lyapunov stability analysis proves that the sinusoidal voltage tracking objective is achieved by the controller with all signals remaining bounded. Experimental results further validate this approach.

9.1 System Model

An H-Bridge inverter with an output LC filter as seen in Fig. 9.1 is used for DC to AC power conversion. Applying the state averaging method, with PWM switching scheme, the average model for an H-Bridge inverter can be written as follows [47]:

$$L\dot{I}_L = V_{in}(D + d_o) - RI_L - V_o \tag{9.1}$$

$$C\dot{V}_o = I_L - I_o \tag{9.2}$$

where L, C, R are the inductance, capacitance and series resistance of the inductance, respectively. V_{in} is the input supply voltage, $D(t)$ is the PWM duty ratio, d_o is a slowly time varying unknown disturbance and $I_L(t)$ is the inductor current. $V_o(t)$, and $I_o(t)$ are the output voltage and output current, respectively. The objective of the control scheme is to design $D(t)$ such that $V_o(t) \to V_d(t)$ as $t \to \infty$, where $V_d(t)$ is the desired sinusoidal output voltage trajectory defined by amplitude, frequency and phase. Taking the derivative of (9.2) and substituting for $\dot{I}_L(t)$ from (9.1) the following second order equation is obtained to represent the system dynamics of the inverter

$$m\ddot{V}_o + a\dot{V}_o + V_o = V_{in}D + V_{in}d_o - RI_o - L\dot{I}_o \tag{9.3}$$

where $m \triangleq LC$ and $a \triangleq RC$.

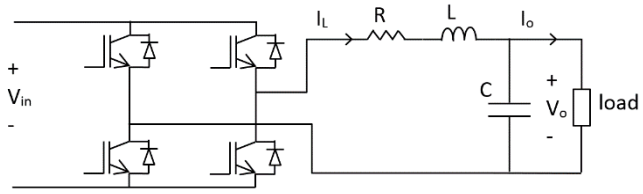

Fig. 9.1 H-Bridge inverter with output LC filter.

9.2 Filter-Based Control Development

In a practical system, the system parameters are subject to change during long term operation for a control scheme in high volume production. Also, parameter tolerance can be a performance issue. To this end, we assume that there are some uncertainties in the values of system parameters, L, C, R, around their nominal values. This can be shown by representing parameter m and a as:

$$\begin{aligned} m &= m_n + \delta m \\ a &= a_n + \delta a \end{aligned} \tag{9.4}$$

where m_n and a_n are calculated based on nominal values of L, C, and R. δm and δa are offsets from nominal values. To facilitate the control development, the following assumptions are made.

Assumption 1: Change of system parameters are limited in a certain range such that:

$$|\delta m| < \overline{m} \tag{9.5}$$

$$|\delta a| < \overline{a} \tag{9.6}$$

where $\overline{m}$ and $\overline{a}$ are upper bounds and $\overline{m} < m_n$.

Assumption 2: The rate of change of m with time is limited such that:

$$|\dot{m}(t)| < \overline{M}. \tag{9.7}$$

Assumption 3: The output voltage $V_o(t)$ is measurable and the input voltage V_{in} is known and constant.

Assumption 4: The disturbance is unknown and slowly time-varying in the sense that $\dot{d}_0 \approx 0$.

Assumption 5: The load current and disturbance have the following properties: $I_o(t), \dot{I}_o(t), d_o(t) \epsilon \mathcal{L}_\infty$.

Assumption 6: The desired voltage trajectory and its first and second time derivatives are known and bounded, i.e. $V_d(t), \dot{V}_d(t), \ddot{V}_d(t) \in \mathcal{L}_\infty$.

To facilitate the controller development and characterize its performance, the tracking error signal $e(\mathrm{t})$ and filtered error signal, $r_f(t)$, are defined as follows:

$$e \triangleq V_d - V_o \tag{9.8}$$

$$\dot{p} \triangleq -K_1 r_f + (K_2 + \alpha)\left(\alpha e - r_f\right) - e - e_f \tag{9.9}$$

$$r_f \triangleq p + (K_2 + \alpha)e \tag{9.10}$$

where K_1, K_2, α are positive gains, $p(t)$ is an auxiliary variable defined for filter implementation and $e_f(t)$ is defined with the following differential equation

$$\dot{e_f} \triangleq -\alpha e_f + r_f. \tag{9.11}$$

To further the control development the following error signal is also defined:

$$\eta \triangleq \dot{e} + \alpha e - r_f. \tag{9.12}$$

Taking derivative of (9.10) and using (9.9) and (9.12) results in:

$$\dot{r_f} = -K_1 r_f + (K_2 + \alpha)\eta - e - e_f. \tag{9.13}$$

Taking derivative of (9.12) and utilizing (9.12), (9.13) and the second derivative of (9.8) after some mathematical simplifications results in the following error dynamic:

$$\dot{\eta} = \ddot{V}_d - \ddot{V}_o + (K_1 + \alpha)r_f - K_2\eta - \alpha^2 e + e + e_f. \tag{9.14}$$

Multiplying both sides of (9.14) by m and substituting for $m\ddot{V}_o$ from (9.3), we get the open loop error dynamic equation (9.15) where (9.8) and (9.12) have been utilized:

$$\begin{aligned} m\dot{\eta} = {} & m\ddot{V}_d + m(K_1 + \alpha)r_f - mK_2\eta - m\alpha^2 e + m(e + e_f) + a\dot{V}_d + a\alpha e \\ & - ar_f - a\eta + V_o - V_{in}D - V_{in}d_o + RI_o + L\dot{I}_o. \end{aligned} \tag{9.15}$$

From (9.15) and motivated by the subsequent stability analysis the duty ratio control signal is defined as:

$$\begin{aligned} D \triangleq \frac{1}{V_{in}} [& m_n\ddot{V}_d + m_n(K_1 + \alpha)r_f - m_n\alpha^2 e + m_n(e + e_f) + a_n\dot{V}_d + a_n\alpha e \\ & -a_n r_f + V_d + (K_2 + \alpha)r_f - V_{in}\hat{d}_0 + K_3 sgn(e - e_f)] \end{aligned} \tag{9.16}$$

where K_3 is a positive constant gain, $sgn(.)$ is the standard signum function and $\hat{d}_0$ is the estimated disturbance with the following estimation error:

$$\tilde{d}_0 \triangleq d_o - \hat{d}_0. \tag{9.17}$$

Finally the closed loop error system is obtained by substituting (9.16) in (9.15) to yield the following:

$$\begin{aligned} m\dot{\eta} = N_1 + \widetilde{N} - mK_2\eta - a\eta - e - (K_2 + \alpha)r_f - V_{in}\tilde{d}_0 \\ - K_3 sgn(e - e_f) \\ -\frac{1}{2}\dot{m}\eta \end{aligned} \tag{9.18}$$

With N_1 and $\widetilde{N}$ defined as:

$$N_1 \triangleq \delta m\ddot{V}_d + \delta a\dot{V}_d + RI_o + L\dot{I}_o \tag{9.19}$$

$$\widetilde{N} \triangleq \delta m(K_1 + \alpha)r_f - \delta m\alpha^2 e + \delta m(e + e_f) + \delta a\alpha e - \delta a r_f + \frac{1}{2}\dot{m}\eta \tag{9.20}$$

where $\frac{1}{2}\dot{m}\eta$ is added to and subtracted from the right hand side of (9.18).

Motivated by the subsequent stability analysis the update law for $\hat{d}_0$is defined as:

$$\dot{\hat{d}}_0 \triangleq -K_4\eta V_{in} \tag{9.21}$$

where K_4 is a positive constant gain. As can be inferred from (9.12), $\eta(t)$ is not a measurable signal. But by substituting for $\eta(t)$ from (9.12) and taking the integral of (9.21) the update law for $\hat{d}_0$ becomes realizable as:

$$\hat{d}_0(t) = -K_4 V_{in}\left[\int_0^t \left(\alpha e(\tau) - r_f(\tau)\right)d\tau + e(t) - e(0)\right] \tag{9.22}$$

9.2.1 Stability Analysis

Before stating the main theorem, the following lemma is presented to be invoked later.

Lemma 1: Let the auxiliary function $L(t)$ be defined as follows:

$$L(t) \triangleq \eta(N_1 - K_3 sgn(e - e_f)) \tag{9.23}$$

If K_3 is selected to meet the following gain condition:

$$K_3 > (|N_1| + \frac{1}{\alpha}|\dot{N}_1|) \tag{9.24}$$

then

$$\int_0^t L(\tau)d\tau \leq \zeta \tag{9.25}$$

where the positive constant ζ is defined as:

$$\zeta \triangleq |e(0)N_1(0)| + K_3|e(0)|. \tag{9.26}$$

Proof: The proof of Lemma1although essentially contained in [70], is given in Appendix A for the sake of completeness.

Theorem 1: Using the closed loop error system equation found in (9.18) the error signals defined in (9.8), (9.10), (9.11) and (9.12) are regulated as follows:

$$e(t), e_f(t), r_f(t), \eta(t) \to 0 \text{ as } t \to \infty.$$

Proof: A non-negative Lyapunov function $S(t) \in \mathbb{R}$ is defined as

$$S \triangleq \frac{1}{2}e^2 + \frac{1}{2}e_f^2 + \frac{1}{2}r_f^2 + \frac{1}{2}m\eta^2 + \frac{1}{2K_4}\tilde{d}_0^2 + \zeta - \int_0^t L(\tau)d\tau. \tag{9.27}$$

Taking the derivative of (9.27) with respect to time and substituting $\dot{e}_f(t), \dot{e}(t), \dot{r}_f(\mathrm{t})$ and $m\dot{\eta}(t)$ from (9.11), (9.12), (9.13) and (9.18), respectively, after some mathematical simplifications the expression in (9.28) is obtained where (9.17), (9.21) and (9.23) are also utilized.

$$\dot{S} = -\alpha e^2 - \alpha e_f^2 - K_1 r_f^2 - K_2 m\eta^2 - a\eta^2 + \tilde{N}\eta \tag{9.28}$$

To proceed we next need to find an upper bound for $\left|\tilde{N}\right|$

$$\begin{aligned}\left|\tilde{N}\right| &\leq [\bar{m}(K_1+\alpha)+\bar{a}]\left|r_f\right| + \bar{m}\left|e_f\right| + [\bar{m}\alpha^2 + \bar{m} + \bar{a}\alpha]|e| + \\ \tfrac{1}{2}\overline{M}|\eta| &= b_1\left|r_f\right| + b_2\left|e_f\right| + b_3|e| + b_4|\eta|\end{aligned} \tag{9.29}$$

where $b_1 \triangleq [\bar{m}(K_1+\alpha)+\bar{a}]$, $b_2 \triangleq \bar{m}$, $b_3 \triangleq [\bar{m}\alpha^2 + \bar{m} + \bar{a}\alpha]$ and $b_4 \triangleq \frac{1}{2}\overline{M}$.

Assuming $K_2 = \frac{1}{m_n - \bar{m}}(K_{21} + K_{22} + K_{23} + K_{24})$ where the auxiliary gains $K_{21}, K_{22}, K_{23}, K_{24}$ are all positive and using (9.29), $\dot{S}(t)$ can be upper bounded as:

$$\begin{aligned}\dot{S} \leq -\alpha e^2 - \alpha e_f^2 - K_1 r_f^2 - a\eta^2 + \left[b_1|\eta|\left|r_f\right| - K_{21}\eta^2\right] + \\ \left[b_2|\eta|\left|e_f\right| - K_{22}\eta^2\right] + [b_3|\eta||e| - K_{23}\eta^2] + (b_4 - K_{24})\eta^2.\end{aligned} \tag{9.30}$$

The three bracketed terms in (9.30), each represent a nonlinear damping pair which can be separately upper bounded as (9.31)-(9.33) [71].

$$b_1|\eta|\left|r_f\right| - K_{21}\eta^2 \leq \frac{b_1^2 {r_f}^2}{K_{21}} \tag{9.31}$$

$$b_2|\eta|\left|e_f\right| - K_{22}\eta^2 \leq \frac{b_2^2 {e_f}^2}{K_{22}} \tag{9.32}$$

$$b_3|\eta||e| - K_{23}\eta^2 \leq \frac{b_3^2 e^2}{K_{23}} \tag{9.33}$$

Assuming the gain conditions (9.34)-(9.37) are meet, $\dot{S}(t)$ can be upper bounded as (9.38).

$$K_{21} > \frac{b_1^2}{K_1} \tag{9.34}$$

$$K_{22} > \frac{b_2^2}{\alpha} \tag{9.35}$$

$$K_{23} > \frac{b_3^2}{\alpha} \tag{9.36}$$

$$K_{24} > b_4 \tag{9.37}$$

$$\dot{S} \leq -\beta_1 r_f^2 - \beta_2 e_f^2 - \beta_3 e^2 - \beta_4 \eta^2 \tag{9.38}$$

Where $\beta_1 \triangleq K_1 - \frac{b_1^2}{K_{21}}$, $\beta_2 \triangleq \alpha - \frac{b_2^2}{K_{22}}$, $\beta_3 \triangleq \alpha - \frac{b_3^2}{K_{23}}$ and $\beta_4 \triangleq K_{24} - b_4 + a$ are positive constants.

From (9.27) and (9.38) it is clear that $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_2 \cap \mathcal{L}_\infty$ and $\tilde{d}_0 \in \mathcal{L}_\infty$. From (9.8) and the fact that $V_d(t) \in \mathcal{L}_\infty$, therefore $V_o(t) \in \mathcal{L}_\infty$. From (9.17) along with Assumption 5 it is clear that $\hat{d}_0 \in \mathcal{L}_\infty$. Now from (9.16) along with Assumption 6 we can see that all the signals contributed in the definition of $D(t)$ are bounded, therefore $D(t) \in \mathcal{L}_\infty$. From (9.11)-(9.13) along with the previously stated bounding statements it is clear that $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}) \in \mathcal{L}_\infty$. With $\dot{e}(t) \in \mathcal{L}_\infty$, (9.8) can be used to deduce $\dot{V}_o(t) \in \mathcal{L}_\infty$. From (9.3) it can be inferred that $\ddot{V}_o(t) \in \mathcal{L}_\infty$. Hence it is clear that all signals in the closed loop are bounded. From (9.14) it is clear that $\dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$. Since $e(t), e_f(t), r_f(t), \eta(t) \in \mathcal{L}_\infty \cap \mathcal{L}_2$ and $\dot{e}(t)$, $\dot{e_f}(t), \dot{r_f}(\mathrm{t}), \dot{\eta}(\mathrm{t}) \in \mathcal{L}_\infty$, Barbalat's Lemma [49] can be utilized to

prove that $e(t), e_f(t), r_f(t), \eta(t) \rightarrow 0 \ as \ t \rightarrow \infty$. Thus completing the proof of the theorem.

9.3 Experimental Results

The test rig used for verifying the performance of the proposed controller and observers is shown in Fig. 9.2. The NI CompactRIO 9022, with cRIO-9113 chassis and the commercial software LabVIEW are used for implementation of the controller algorithm. The control algorithm is first developed using LabVIEW software on a personal computer and then downloaded to the onboard Virtex-5 LX50 FPGA of the cRIO-9113. The real-time experimental results were sent back to the personal computer through real time controller cRIO-9022 for monitoring and data logging. The dc link is fed by a single phase voltage doubler rectifier. The control algorithm requires only one voltage sensor to measure the output voltage, $V_o(t)$. For the purposes of data logging and visualization two current sensors are also utilized for the output current and inductor current measurement.

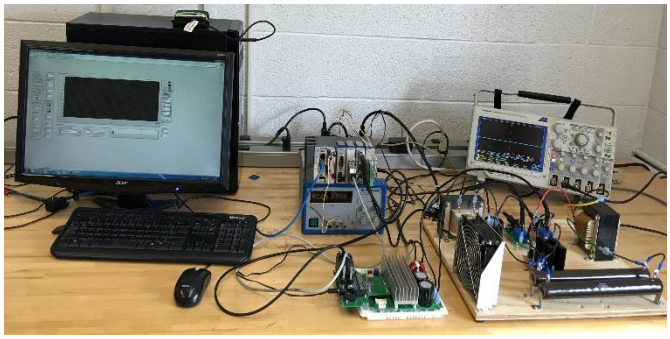

Fig. 9.2 Experimental setup of the H-Bridge inverter.

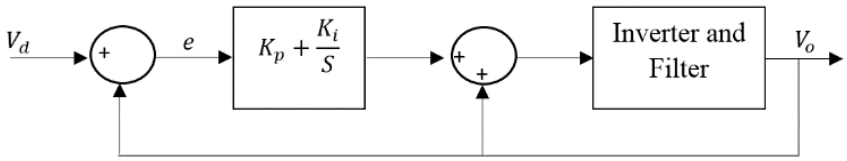

Fig. 9.3 Output feed-forward controller.

The performance of the developed controller is compared with a commonly used output feed-forward controller depicted in Fig. 9.3. For the sake of a fair comparison, the gains of PI block of output feed-forward controller are adjusted so that the two closed-loop control systems have the same transient time and percent overshoot. Therefore, the performance of the controllers can be compared in terms of steady state error. Table 9.1 summarizes the system parameters used for experimental test.

Table 9.1 System Parameters

Inverter Parameter	**Value**	**Proposed Controller Parameters**	**Value**
Output AC voltage	120 [Vrms]	Gain K_1	20
Supply DC voltage, V_{in}	350 [V]	GainK_2	4
Filter inductance, L	10 [mH]	GainK_3	20
Inductor Resistance, R	0.01 [Ω]	GainK_4	1
Filter capacitance, C	50 [μF]	Gainα	2.5
AC Voltage frequency	60 [Hz]		
Switching Frequency	5 [kHz]	**Output Feed-forward Controller Parameters**	**Value**
Load1 Inductance	32 [mH]	K_p	7
Load1 Resistance	37.5 [Ω]	K_i	7
Load2 Capacitance	220 [μF]		
Load2 Resistance	250 [Ω]		
Load2 Crest Factor	3		

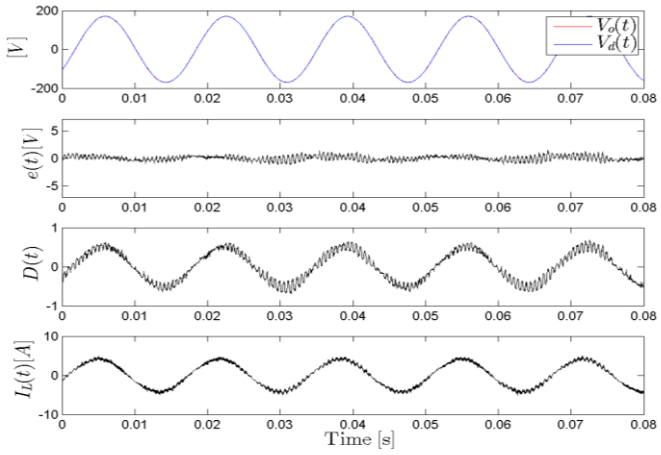

Fig. 9.4 Steady-state response of the filter-based controller under RL load.

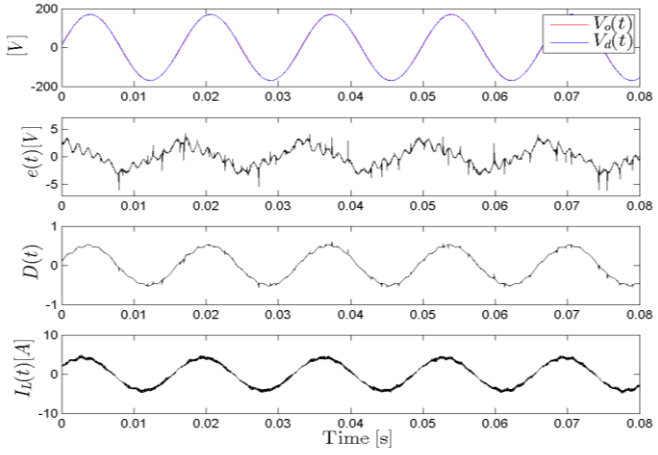

Fig. 9.5 Steady-state response of the output feed-forward controller under RL load.

In the first study, the steady state performance of the proposed control schemes under linear resistive-inductive load is investigated. Fig. 9.4 and 9.5, show the desired, $V_d(t)$, and actual, $V_o(t)$, output voltage, tracking error, $e(t)$, and the inductor current, $I_L(t)$, as well as the control signal, $D(t)$, for the proposed control scheme and output feed-forward controller, respectively. As can be seen in these figures, the filter-based control scheme outperforms the output feed-forward controller in voltage tracking and an excellent

reference tracking with the steady-state peak error less than 0.6% is achieved for the proposed control scheme. The steady state error of the output feed-forward controller is measured as 2%.

In a second study the transient response to a -50% step change in amplitude of reference voltage, $V_d(t)$, under nominal 37.5 [Ω] resistive load is considered. As it can be seen in Fig. 9.6 and 9.7, to represent the worst case operation, the reference command is changed when the output voltage is at its peak value. As it was mentioned earlier in this section, the gain of output feed-forward controller is selected so that the two control schemes have the same transient time and percent overshoot. This test provides a baseline showing the transient response of both controllers have similar characteristics.

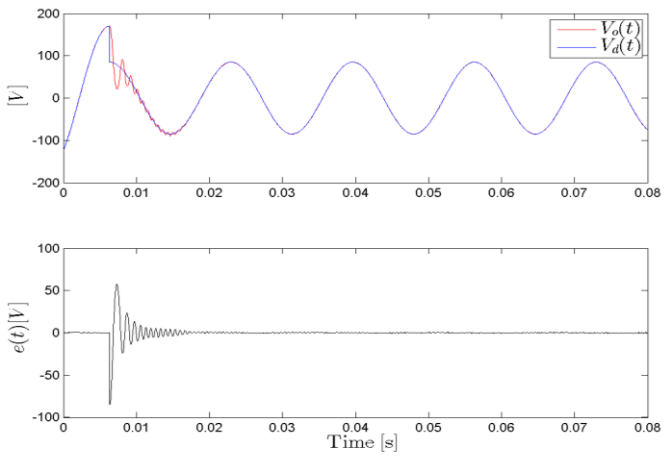

Fig. 9.6 Transient response of the filter-based controller under resistive load.

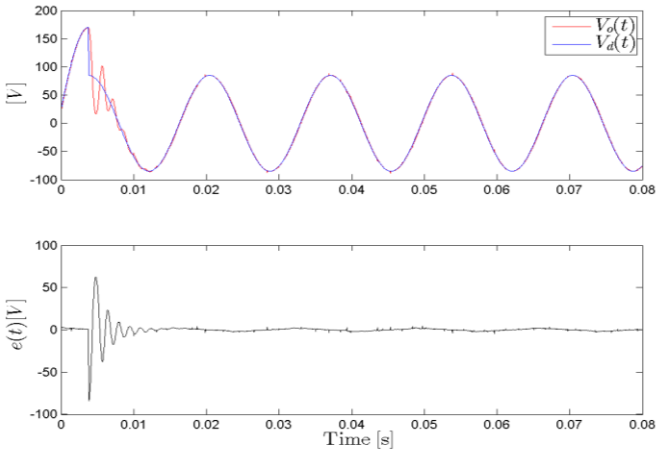

Fig. 9.7 Transient response of the output feed-forward controller under resistive load.

A third study evaluates the performance of the proposed control scheme and the reference output feed-forward controller under a worst case operation scenario where a highly distorting load is used consisting of a full wave rectifier bridge feeding a 250 [Ω] resistor in parallel with a 220 [μF] capacitor. The results under nonlinear rectifier load are illustrated in Fig. 9.8 and 9.9. Despite the highly distorted load current, the output voltage tracking with the steady-state peak error less than 0.76% is achieved for the filter-based controller in comparison with that of 3% of the output feed-forward controller. These results shows that the proposed filter-based controller improves the system performance in terms of steady-state error at least 70% in comparison with the reference output feed-forward controller for both linear and nonlinear loads.

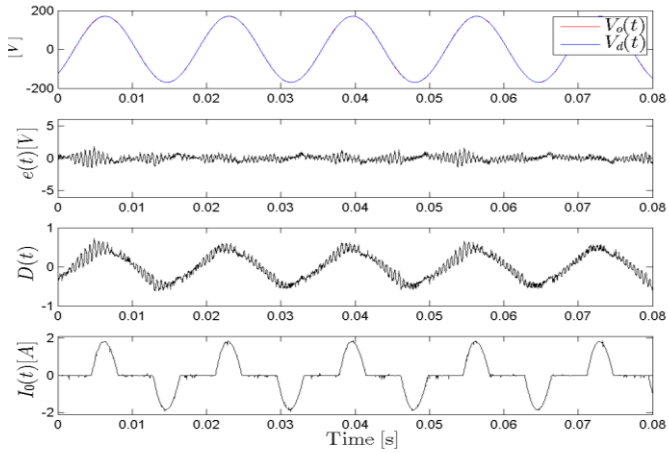

Fig. 9.8 Steady-state response of the filter-based controller under a highly distorting rectifier load.

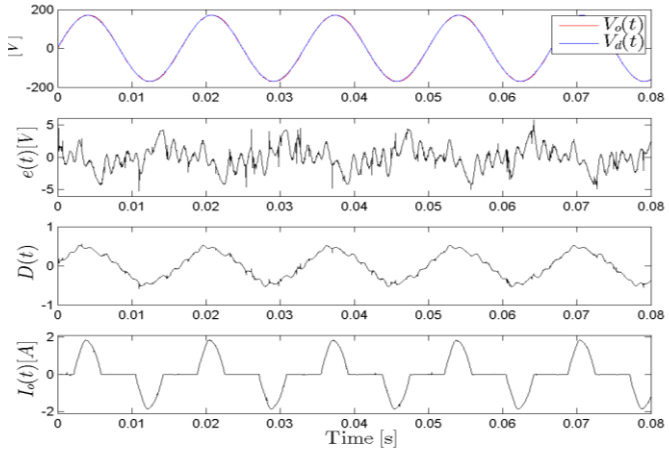

Fig. 9.9 Steady-state response of the output feed-forward controller under a highly distorting rectifier load.

In a final study, the performance of the proposed controller is evaluated under +50% parameter discrepancy for both inductance and capacitance values. To perform this study the nominal value of inductance and capacitance have been considered 15 [mH] and 75 [μF], respectively, in the control law of the filter-based control scheme. Again, an excellent reference tracking with the steady-state peak error less than 0.8% is achieved as shown in

Fig. 9.10 and 9.11. The voltage THD is limited within 0.4% which fulfills IEEE 519 and EN 50160 standards for US and European power systems, respectively.

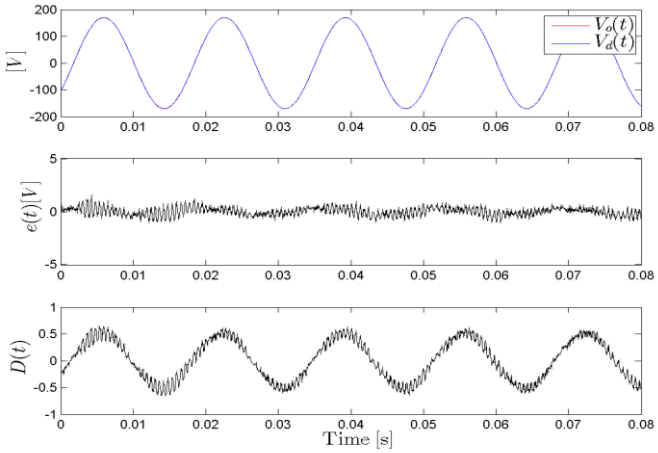

Fig.9.10 Steady-state response of the filter-based controller with +50% inductance discrepancy under RL load.

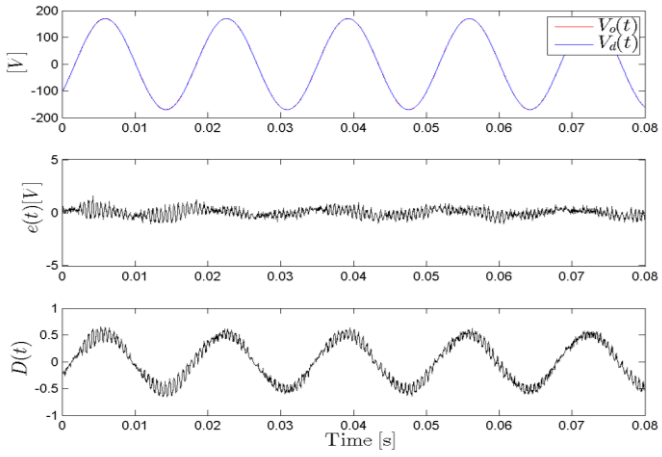

Fig. 9.11 Steady-state response of the filter-based controller with +50% capacitance discrepancy under RL load.

9.4 Summary

In this paper a new filter-based control scheme relying on only a single output voltage measurement was proposed to regulate the instantaneous output voltage of a single-phase inverter in stand-alone mode. The performance of the control scheme is confirmed through experimental results in terms of steady-state tracking error, THD, stability and transient response. In addition to the lower cost resulting from removing current measurement sensors, this scheme has demonstrated its effectiveness in terms of low THD, excellent voltage regulation and insensitivity to load and parameter variations.

CHAPTER 10

CONCLUSION AND FUTURE WORKS

10.1 Conclusion

In this dissertation, nonlinear control techniques, such as backstepping controller and filter-based controller, were utilized for the control of power converters in different applications of DG systems. Key features and important results of each control technique are being summarized in the following.

10.1.1 Backstepping Controller

The first nonlinear control scheme which was developped for the control of a PWM power converter was based on backstepping technique. To overcome the drawbacks of the backstepping controller such as dependency of the control law to the numerical derivative of the noisy current measurement, a combination of the backstepping controller with other control techniques such as output current observer, nonlinear sliding technique, periodic learning and inductor current observer was proposed. Also, the extension of the work for a 3-phase system was developed and discussed in detail. The proposed backstepping

controller was developed in $dq0$-frame for the control of a 3-phase 4-wire diode clamped inverter with output LC filter under different loads including balanced, unbalanced, linear and nonlinear loads. Furthermore, the seamless transition of the inverter from standalone to grid-tie was investigated while the inverter was under the control of the proposed controller. For each developed control scheme, a Lyapunov stability analysis was presented which proved that the voltage tracking objective was achieved by the controller with all signals remaining bounded. Simulation results further validated the proposed approaches.

Comparing the duty ratio control command signals for the backstepping controller combined with a load-current observer and/or a inductor current observer with those of the backstepping controller combined with sliding technique, we realize that the former has a less harsh control command at the cost of greater steady state errors. A periodic learning can untangle both shortfall of the sliding technique and output current observer at the cost of more physical memory required to store one period of the observed disturbance.

10.1.2 Filter-Based Controller

In another effort, filter-based control techniques were developed as effective control schemes which require only single output voltage measurement in their control law. The proposed filter-based control schemes not only eliminate the need for costly current sensors to measure the inductor and/or output currents, but also they are robust against system parameter discrepancy and system disturbances. Our experimental results show that the filter-based control technique utilizing the nominal values of the system parameters and compensate for parameter discrepancies has much better performance than the filter-based controller developed for unknown system parameters. Also, the controller developed for unknown system parameters requires higher gain values to be stabilized. For each

developed control scheme, a Lyapunov stability analysis is presented which proves that the voltage tracking objective is achieved by the controller with all signals remaining bounded. Experimental results further validate the proposed approaches.

10.2 Future Work

Some ideas for future work are mentioned below:

10.2.1 Grid-Tie Mode

Depending on the operation of the power converters in DG systems, power converters can be classified as grid-forming (standalone) or grid-feeding (grid-tie) converters. In the course of the dissertation, we have investigated the control of grid-forming converters designed to generate an output voltage with desired amplitude, phase and frequency. On the other hand, grid-feeding converters are mainly designed to deliver a specific amount of active and reactive power to an energized grid. Control of grid-feeding converters could be a possible extension of this work.

10.2.2 Hierarchical Cooperative Control Scheme and Optimization

Multi-microgrid and Hybrid ac/dc microgrids have been considered for better interconnection of different DG systems to the power grid. As it can be seen in Fig. 10.1, this interconnection is through utilizing interlinking power converters including: dc/dc, dc/ac, ac/ac and ac/dc converters with a proper management and control strategy. The interlinking converters as a subcategory of grid-feeding converters are responsible for transferring a specific amount of active power from one microgrid to the other. In the top layer of a hierarchical control strategy we can solve a centralized optimization problem to

balance the resource utilization among all interconnected microgrids. The output of this optimization problem is the target active (or reactive power) of all grid-forming and subsequently grid-feeding converters. Then in the bottom layer of the control strategy we can apply nonlinear control techniques to meet generation or delivery of these target powers. Applying the nonlinear control techniques developed in this dissertation for the control of grid-forming converters and extending these control algorithms for grid-feeding converters in a multi-microgrid network when the whole network is utilizing an optimization problem in a higher layer could be interesting to investigate.

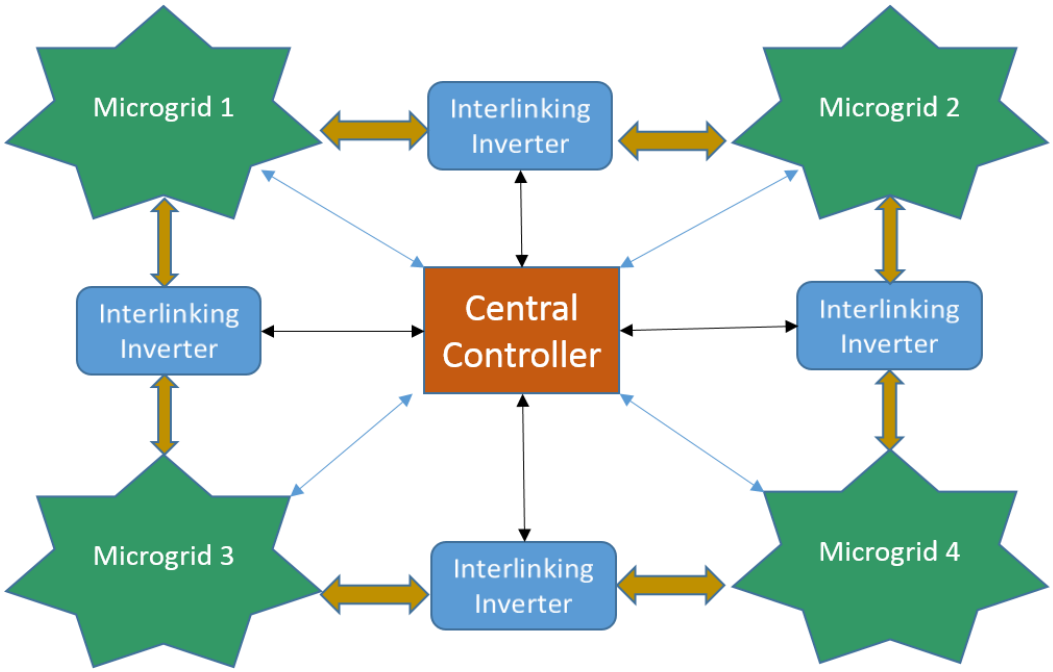

Fig. 10.1 Multi microgrid system.

REFERENCES

[1] H. Gu, Z. Yang, D. Wang and W. Wu, "Research on Control Method of Double-Mode Inverter with Grid-Connection and Stand-Alone," in *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*, Shanghai, 2006.

[2] R. J. Wai, C. Y. Lin, Y. C. Huang and Y. R. Chang, "Design of High-Performance Stand-Alone and Grid-Connected Inverter for Distributed Generation Applications," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 4, pp. 1542-1555, April 2013.

[3] C. Trujillo Rodriguez, D. Velasco de la Fuente, G. Garcera, E. Figueres and J. A. Guacaneme Moreno, "Reconfigurable Control Scheme for a PV Microinverter Working in Both Grid-Connected and Island Modes," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 4, pp. 1582-1595, April 2013.

[4] Z. Yao, L. Xiao and Y. Yan, "Seamless Transfer of Single-Phase Grid-Interactive Inverters Between Grid-Connected and Stand-Alone Modes," *IEEE Transactions on Power Electronics,* vol. 25, no. 6, pp. 1597-1603, June 2010.

[5] M. Schoen and M. McIntyre, "Vehicle to grid as a household backup generator utilizing a novel backstepping controller with uncertain load for full bridge converter," in *4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Rogers, AR, July 2013.

[6] D. Velasco de la Fuente, C. L. Trujillo Rodríguez, G. Garcerá, E. Figueres and R. Ortega Gonzalez, "Photovoltaic Power System With Battery Backup With Grid-Connection and Islanded Operation Capabilities," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 4, pp. 1571-1581, April 2013.

[7] R. Razi and M. Monfared, "Simple control scheme for single-phase uninterruptible power supply inverters with Kalman filter-based estimation of the output voltage," *IET Power Electronics,* vol. 8, no. 9, pp. 1817-1824, 2015.

[8] M. J. Ryan, W. E. Brumsickle and R. D. Lorenz,, "Control topology options for single-phase UPS inverters," in *Power Electronics, Drives and Energy Systems for Industrial Growth, 1996., Proceedings of the 1996 International Conference on*, New Delhi, 1996.

[9] H. Komurcugil, "Improved passivity-based control method and its robustness analysis for single-phase uninterruptible power supply inverters," *IET Power Electronics,* vol. 8, no. 8, pp. 1558-1570, 2015.

[10] G. Willmann, D. F. Coutinho, L. F. A. Pereira and F. B. Libano, , "Multiple-Loop H-Infinity Control Design for Uninterruptible Power Supplies," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 3, pp. 1591-1602, June 2007.

[11] G. Bonan, O. Mano, L. F. A. Pereira and D. F. Coutinho, "Robust control design of multiple resonant controllers for sinusoidal tracking and harmonic rejection in Uninterruptible Power Supplies," in *IEEE International Symposium on Industrial Electronics*, Bari, 2010.

[12] Keliang Zhou and Yunhu Yang, "Phase compensation multiple resonant control of single-phase PWM inverter," in *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*, Hangzhou, 2012.

[13] S. Buso, S. Fasolo and P. Mattavelli, "Uninterruptible power supply multiloop control employing digital predictive voltage and current regulators," *IEEE Transactions on Industry Applications,* vol. 37, no. 6, pp. 1846-1854, 2001.

[14] Poh Chiang Loh, M. J. Newman, D. N. Zmood and D. G. Holmes, "A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems," *IEEE Transactions on Power Electronics,* vol. 18, no. 5, pp. 1176-1185, 2003.

[15] Poh Chiang Loh and D. G. Holmes, "Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters," *IEEE Transactions on Industry Applications,* vol. 41, no. 2, pp. 644-654, 2005.

[16] P. Mattavelli, "An improved deadbeat control for UPS using disturbance observers," *IEEE Transactions on Industrial Electronics,* vol. 52, no. 1, pp. 206-212, Feb. 2005.

[17] Kai Zhang, Yong Kang, Jian Xiong and Jian Chen, "Direct repetitive control of SPWM inverter for UPS purpose," *in IEEE Transactions on Power Electronics,* vol. 18, no. 3, pp. 784-792, May 2003.

[18] T. Haneyoshi, A. Kawamura and R. G. Hoft, "Waveform compensation of PWM inverter with cyclic fluctuating loads," *IEEE Transactions on Industry Applications,* vol. 24, no. 4, pp. 582-589, 1988.

[19] K. Zhang, Li Peng, J. Xiong and J. Chen. , "State-feedback-with-integral Control plus Repetitive Control for PWM Inverters," in *CSEE*, 2006.

[20] Ying-Yu Tzou, Shih-Liang Jung and Hsin-Chung Yeh, "Adaptive repetitive control of PWM inverters for very low THD AC-voltage regulation with unknown loads," *IEEE Transactions on Power Electronics,* vol. 14, no. 5, pp. 973-981, Sep 1999.

[21] C. Rech, H. A. Grundling and J. R. Pinheiro, "A modified discrete control law for UPS applications," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, Galway, 2000.

[22] C. Rech, H. Pinheiro, H. A. Grundling, H. L. Hey and J. R. Pinheiro,, "Comparison of digital control techniques with repetitive integral action for low cost PWM inverters," *IEEE Transactions on Power Electronics,* vol. 18, no. 1, pp. 401-410, Jan 2003.

[23] Ying-Yu Tzou, Rong-Shyang Ou, Shih-Liang Jung and Meng-Yueh Chang, "High-performance programmable AC power source with low harmonic distortion using DSP-based repetitive control technique," *IEEE Transactions on Power Electronics,* vol. 12, no. 4, pp. 715-725, Jul 1997.

[24] Keliang Zhou, Kay-Soon Low, D. Wang, Fang-Lin Luo, Bin Zhang and Yigang Wang, "Zero-phase odd-harmonic repetitive controller for a single-phase PWM inverter," *IEEE Transactions on Power Electronics,* vol. 21, no. 1, pp. 193-201, Jan. 2006.

[25] A. Roshan, R. Burgos, A. C. Baisden, F. Wang and D. Boroyevich, "A D-Q Frame Controller for a Full-Bridge Single Phase Inverter Used in Small Distributed Power Generation Systems," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, Anaheim, CA, USA, 2007.

[26] D. Dong, T. Thacker, R. Burgos, F. Wang and D. Boroyevich, "On Zero Steady-State Error Voltage Control of Single-Phase PWM Inverters With Different Load Types," *IEEE Transactions on Power Electronics,* vol. 26, no. 11, pp. 3285-3297, Nov. 2011.

[27] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions on Power Electronics,* vol. 18, no. 3, pp. 814-822, May 2003.

[28] A. Kawamura and T. Yokoyama, "Comparison of five different approaches for real time digital feedback control of PWM inverters," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*, Seattle, WA, USA, 1990.

[29] Shih-Liang Jung, Meng-Yueh Chang, Jin-Yi Jyang, Li-Chia Yeh and Ying-Yu Tzou, "Design and implementation of an FPGA-based control IC for AC-voltage regulation," *IEEE Transactions on Power Electronics,* vol. 14, no. 3, pp. 522-532, , May 1999.

[30] P. Mattavelli, G. Escobar and A. M. Stankovic, "Dissipativity-based adaptive and robust control of UPS," *IEEE Transactions on Industrial Electronics,* vol. 8, no. 2, pp. 334-343, 2001.

[31] G. Escobar, A. M. Stankovic and P. Mattavelli, "Dissipativity-based adaptive and robust control of UPS in unbalanced operation," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, Vancouver, BC, 2001.

[32] G. E. Valderrama, A. M. Stankovic and P. Mattavelli, "Dissipativity-based adaptive and robust control of UPS in unbalanced operation," *IEEE Transactions on Power Electronics,* vol. 18, no. 4, pp. 1056-1062, July 2003.

[33] P. C. Tan, P. C. Loh and D. G. Holmes, "High-Performance Harmonic Extraction Algorithm for a 25 kV Traction Power Quality Conditioner," *IEE*

Proceedings - Electric Power Applications, vol. 151, no. 5, pp. 505-512, Sept. 2004.

[34] M. Monfared, S. Golestan and J. M. Guerrero, "Analysis, Design, and Experimental Verification of a Synchronous Reference Frame Voltage Control for Single-Phase Inverters," *IEEE Transactions on Industrial Electronics,,* vol. 61, no. 1, pp. 258-269, Jan. 2014.

[35] M. Dai, M. N. Marwali, J. W. Jung and A. Keyhani, "A Three-Phase Four-Wire Inverter Control Technique for a Single Distributed Generation Unit in Island Mode," *IEEE Transactions on Power Electronics,* vol. 23, no. 1, pp. 322-331, Jan. 2008.

[36] Hong Yi, Jiyang Dai and Jiaju Wu, "Research on modeling and control of the single-phase inverter system with a nonlinear load," in *Intelligent Control and Automation, 2008. WCICA 2008. 7th World Congress on*, Chongqing, 2008.

[37] Tsang-Li Tai and Jian-Shiang Chen, "UPS inverter design using discrete-time sliding-mode control scheme," *IEEE Transactions on Industrial Electronics,* vol. 49, no. 1, pp. 67-75, Feb 2002.

[38] R. Majdoul, E. Abdelmounim, M. Aboulfatah and A. Abouloifa, "The Performance comparative of Backstepping, Sliding Mode and PID controllers designed for a single-phase inverter UPS," in *Multimedia Computing and Systems (ICMCS), 2014 International Conference on,*, Marrakech, 2014.

[39] M. J. Ryan, W. E. Brumsickle and R. D. Lorenz, "Control topology options for single-phase UPS inverters," *IEEE Transactions on Industry Applications,* vol. 33, no. 2, pp. 493-501, 1997.

[40] N. M. Abdel-Rahim and J. E. Quaicoe, "Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters," *IEEE Transactions on Power Electronics,* vol. 11, no. 4, pp. 532-541, Jul 1996.

[41] M. J. Ryan and R. D. Lorenz, "A high performance sine wave inverter controller with capacitor current feedback and "back-EMF" decoupling," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, Atlanta, GA, 1995.

[42] W. Kempton, J. Tomić, "Vehicle to Grid Implementation: from stabilizing the grid to supporting large-scale renewable energy," *J. Power Sources,* vol. 144, no. 1, pp. 280-294, 1 June 2005.

[43] M. Mohebbi, M. L. McIntyre and J. Latham, "Vehicle to grid utilizing a backstepping controller for bidirectional full-bridge converter and five level active neutral point inverter," in *IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015.

[44] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke and N. Celanovic, "Active Neutral-Point-Clamped Multilevel Converters," in *2005 IEEE 36th Power Electronics Specialists Conference*, Jun. 2005.

[45] M. Mohebbi, M. L. McIntyre, J. F. Naber and R. Hickman, "13.8 kV five level ANPC inverter for wind power," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014.

[46] H. Sira-Ramirez , R. Perez-Moreno, R. Ortega, M. Garcia-Esteban , "Passivity-based Controllers for the stabilisation of DC-to-DC power converters," *Automatica,* 1997.

[47] R. Middlebrook, "A general unified approach to modeling switching converter power stages," *Int. J. Electronics,* vol. 42, pp. 521-550, 1997.

[48] V. M. Rao, A. K. Jain, K. K. Reddy and A. Behal, "Nonlinear Control of a Single Phase Unity Power Factor Rectifier: Design, Analysis, and Experimental Results," *IEEE Transactions on Control Systems Technology,* vol. 16, no. 6, pp. 1301-1307, Nov. 2008.

[49] J. Slotine and W. Li, Applied Nonlinear Control, Englewood Cliffs, NJ: Prentice Hall, 1991.

[50] Mohan, Undeland, Robbins, Power Electronics: converters, applications and design , Singapore, John Wiley and sons,1989,book., Singapore: John Wiley and sons, 1989.

[51] G. Hua and F. C. Lee, "Soft-switching PWM techniques and their applications," in *Power Electronics and Applications, 1993., Fifth European Conference on*, Brighton, 1993.

[52] Dong-Choon Lee and G-Myoung Lee, "Linear control of inverter output voltage in overmodulation,," *IEEE Transactions on Industrial Electronics,* vol. 44, no. 4, pp. 590-592, Aug 1997.

[53] N. Mohan, T. M. Undeland and W. P., Power Electronics, John Wiley & Sons, 2003.

[54] S. Chen, Y. M. Lai, S. C. Tan and C. K. Tse, "Fast response low harmonic distortion control scheme for voltage source inverters," *IET Power Electronics,* vol. 2, no. 5, pp. 574-584, Sept. 2009.

[55] F. J. Chang, E. C. Chang, T. J. Liang and J. F. Chen, "Digital-signal-processor-based DC/AC inverter with integral-compensation terminal sliding-mode control," *IET Power Electronics,* vol. 4, no. 1, pp. 159-167, January 2011.

[56] L. Schirone, F. Celani and M. Macellari, "Discrete-time control for DC-AC converters based on sliding mode design,," *IET Power Electronics,* vol. 5, no. 6, pp. 833-840, July 2012.

[57] M. Mohebbi, M. L. McIntyre and J. Latham, "Energy efficient DC to AC power conversion using advanced controllers and novel voltage trajectories," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015.

[58] D. Hart, Power Electronics, McGraw Hill, 2011.

[59] M. N. Marwali and A. Keyhani, "Control of distributed generation systems-Part I: Voltages and currents control," *IEEE Transactions on Power Electronics,* vol. 19, no. 6, pp. 1541-1550,, 2004.

[60] M. Kojima, K. Hirabayashi, Y. Kawabata, E. C. Ejiogu and T. Kawabata, "Novel vector control system using deadbeat controlled PWM inverter with output LC filter," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the,*, Pittsburgh, PA, USA, , 2002.

[61] Xuejuan Kong, Jingjiang Wang, Li Peng, Yong Kang and Jian Cheng, "The control technique of three-phase voltage-source inverter output waveform based on internal model theory," in *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, 2003.

[62] M. Mohebbi, M. L. McIntyre and J. Latham, "A learning backstepping controller for voltage source inverter with nonlinear loads," in *IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, 2017.

[63] W. Messner, R. Horowitz, W. W. Kao and M. Boals, "A new adaptive learning rule," *IEEE Transactions on Automatic Control,* vol. 36, no. 2, pp. 188-197, 1991.

[64] M. Mohebbi, M. L. McIntyre, J. Latham and P. Rivera, "Nonlinear control of standalone inverter with unbalanced, nonlinear load," in *IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, 2017.

[65] M. Mohebbi, M. L. McIntyre and J. Latham, "A backstepping controller for voltage source inverter with inductor current and output current observers," in *IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, 2017.

[66] P. Cortes, G. Ortiz, J. I. Yuz, J. Rodriguez, S. Vazquez and L. G. Franquelo, "Model Predictive Control of an Inverter With Output LC Filter for UPS Applications," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 6, pp. 1875-1883, 2009.

[67] M. Mohebbi, M. L. McIntyre, J. Latham and P. Rivera, "A filter-based controller for a buck converter," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017.

[68] M. Mohebbi, J. Latham, M. L. McIntyre and P. Rivera, "Filter-based control of an H-Bridge inverter with output LC filter," in *American Control Conference (ACC)*, Seattle, WA, 2017.

[69] B. Xian, M. S. Queiroz, D. M. Dawson, and M. L. McIntyre, "A discontinuous output feedback controller and velocity observer for nonlinear mechanical systems," *Automatica,* vol. 40, no. 4, p. 695–700, 2004.

[70] B. Xian, M. S. de Queiroz, D. M. Dawson and M. L. McIntyre, "Output feedback variable structure-like control of nonlinear mechanical systems," in *Decision and Control*, Maui, HI, USA , 2003.

[71] M. Krstic, I. Kanellakopoulos, and P. Kokotovic, Nonlinear and Adaptive Control Design, John Wiley & Sons, 1995.

[72] M. Mohebbi, Joseph Latham, Michael McIntyre, Pablo Rivera, "Filter-Based Control of an H-Bridge Inverter with Output LC Filter," in *Proceedings of the 2017 American Control Conference, ACC*, Seattle, WA,, 2017.

[73] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications,* Vols. IA-17, no. 5, pp. 518-523, 1981.

[74] M. Khazraei, H. Sepahvand, K. Corzine and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, Palm Springs, CA, 2010.

[75] H. Iman Eini, Sh. Farhangi, and J.L. Schanen, "A modular AC/DC rectifer based on cascaded H-bridge rectifer," in *Power Electronics and Motion Control Conference, 2008 EPE-PEMC*, sept. 2008.

[76] [Online]. Available: http://www.plexim.com/.

[77] M. R. Islam, Y. Guo and J. Zhu, "A transformer-less compact and light wind turbine generating system for offshore wind farms," in *Power and Energy (PECon), 2012 IEEE International Conference on*, Kota Kinabalu, 2012.

APPENDIX A

After substituting η from (9.12) into (9.23) and integrating in time, we get (a.1) where (9.11) is also utilized.

$$\int_0^t L(\tau)d\tau = \int_0^t \left(\dot{e}(\tau) + \alpha e(\tau) - \dot{e_f}(\tau) - \alpha e_f(\tau)\right)\left(N_1(\tau) - K_3 sgn\left(e(\tau) - e_f(\tau)\right)\right)d\tau \tag{a.1}$$

Defining new variable $w(t) \triangleq e(t) - e_f(t)$ and substituting into (a.1), simplifies (a.1) as:

$$\begin{aligned}\int_0^t L(\tau)d\tau &= \int_0^t \left(\alpha w(\tau) + \dot{w}(\tau)\right)\left(N_1(\tau) - K_3 sgn\big(w(\tau)\big)\right)d\tau \\ &= \int_0^t \alpha w(\tau)\left(N_1(\tau) - K_3 sgn\big(w(\tau)\big)\right)d\tau \\ &+ \int_0^t \dot{w}(\tau)\left(N_1(\tau) - K_3 sgn\big(w(\tau)\big)\right)d\tau.\end{aligned} \tag{a.2}$$

The last integral in (a.2) can be calculated as:

$$\int_0^t \dot{w}(\tau)\left(N_1(\tau) - K_3 sgn\big(w(\tau)\big)\right)d\tau = w(\tau)N_1(\tau)\Big|_0^t - K_3|w(\tau)|\Big|_0^t - \int_0^t w(\tau)\dot{N}_1(\tau)\,d\tau. \tag{a.3}$$

Substituting (a.3) into (a.2) we obtain:

$$\begin{aligned}\int_0^t L(\tau)d\tau = \; & w(\tau)N_1(\tau)\Big|_0^t - K_3|w(\tau)|\Big|_0^t \\ & + \int_0^t w(\tau)\left(\alpha N_1(\tau) - \dot{N}_1(\tau) - \alpha K_3 sgn\big(w(\tau)\big)\right)d\tau.\end{aligned} \tag{a.4}$$

Assuming the gain condition (9.24), the integral of $L(t)$ can be upper bounded as (a.5) with $e_f(0) = 0$.

$$\int_0^t L(\tau)d\tau \leq |w(t)|(|N_1(t)| - K_3) + |w(0)N_1(0)| + K_3|w(0)|$$

$$+ \int_0^t |w(\tau)|\left(\alpha|N_1(\tau)| + \left|\dot{N}_1(\tau)\right| - \alpha K_3\right) d\tau \tag{a.5}$$

$$\leq |e(0)N_1(0)| + K_3|e(0)| = \zeta$$

Thus completing the proof of the Lemma 1.

CURRICULUM VITAE

Mohammad Mohebbi

mohammad.mohebbi@louisville.edu

ADDRESS

207 WS Speed Hall, University of Louisville, Louisville, KY 40292

(662) 380-3795

EDUCATION

- **PhD**. Electrical Engineering, 2013-2017.
  (Power Electronics and Control Systems)
  The University of Louisville, Louisville, KY
  GPA: 3.96.

- **M.Sc.** Electrical Engineering, 2002-2005.
  (Telecommunication Systems)
  Iran University of Science & Technology, Tehran
  GPA: 3.44.

- **B.Sc.** Electrical Engineering, 1998-2002.
  (Electronics)
  Tehran Polytechnic (Amirkabir University of Technology), Tehran
  GPA: 3.42.

HONORS AND AWARDS

- National Instruments (NI) Academic Research Grant Program, 2017.
- Electrical Engineering Outstanding Graduate Student Award, University of Louisville, 2016.
- 2nd place Graduate Research Award, 102nd Kentucky Academy of Science, 2016.

- Martha and Frank Diebold Award to Inspire Engineering for Change, University of Louisville, 2015.
- Student Research Competition Award, University of Louisville, 2015.
- Theobald Scholarship Award, University of Louisville, 2015.
- School of Interdisciplinary and Graduate Studies Tuition Match, University of Louisville, 2015.
- Speed NR Waiver, University of Louisville, 2015.
- Research Tuition Award, University of Louisville, 2014.
- School of Interdisciplinary and Graduate Studies Tuition Match, University of Louisville, 2014.
- Speed NR Waiver, University of Louisville, 2014.
- Several Conferences Travel Award.
- Ranked 3rd in B.Sc. among electrical engineering students, Amirkabir University of Technology, 2002.

INTERESTS

- Intelligent Control through Learning and Optimization,
- Data Analysis,
- Nonlinear Control Theory and Application,
- Model Predictive Control,
- Parameter Estimation, System Identification, System Dynamic Observation and Fault Detection Schemes,
- Microgrid, Smart Grid, and Renewable Energy Systems,
- Computer Programming.

PATENT

M. Mohebbi, M. L. McIntyre, S. Kusumba, G. W. Hahn, Method for Operating a Linear Compressor, U.S. Patent No. US20170122309 A1, May 4, 2017.

PUBLICATIONS

Book Chapter:

1. **M. Mohebbi**, N. M. Moghadam, ICI Reduction Methods in OFDM Systems, *Recent Advances in Wireless Communications and Networks, Jia-Chin Lin (Ed.), ISBN: 978-953-307-274-6, InTech, 2011.*

Peer Reviewed Journal Paper:

1. Joseph Latham, Michael McIntyre, and **M. Mohebbi**, Sensorless Resonance-tracking and Stroke Control of a Linear Vapor Compressor via Nonlinear

Observers, Accepted for publication in a future issue of , *IEEE Transaction on Industrial Electronics.*

2. **M. Mohebbi**, M. L. McIntyre, J. Latham, Impact Fault Detection for Linear Vapor Compressor Using RISE Observer, in *IEEE Transactions on Control Systems Technology* , vol. PP, no.99, pp.1-8, Apr. 2017.
3. Joseph Latham, Michael McIntyre, and **M. Mohebbi,** Parameter Estimation and a Series of Nonlinear Observers for the System Dynamics of a Linear Vapor Compressor, *IEEE Transaction on Industrial Electronics*, vol. 63, no. 11, pp. 6736-6744, Nov. 2016.

Under Preparation:

1. **M. Mohebbi**, Michael McIntyre, Joseph Latham, Sensorless Control of an H-Bridge Inverter with Output LC Filter, To be published, *IET Power Electronics.*
2. **M. Mohebbi**, Michael McIntyre, Joseph Latham, Sensorless Speed Control of DC Servo Motor Using RISE Observer and Filter-Based Controller, under preparation, *IEEE Transaction on Power Systems*.

Conference Paper:

1. P. R. Rivera, M. L. McIntyre, **M. Mohebbi**, and J. Latham, Single-Stage, Single-Phase Grid-Connected Photovoltaic System with Current Ripple Mitigation based on Nonlinear Control, Accepted, *IEEE International Conference on Energy and Environment, CIEM 2017*.
2. Pablo Rivera A., Michael McIntyre, **M. Mohebbi** and Joseph Latham, Single-Stage Three-Phase Grid-Connected Photovoltaic System with Maximum Power Tracking and Active and Reactive Power Control based on Nonlinear Control, Accepted, *2017 IEEE Energy Conversion Congress and Exposition (ECCE).*
3. **M. Mohebbi**, Joseph Latham, Michael McIntyre, Pablo Rivera, Filter-Based Control of an H-Bridge Inverter with Output LC Filter, *Proceedings of the 2017 American Control Conference, ACC*, Seattle, WA, 2017, pp. 4075-4080.
4. Joseph Latham, **M. Mohebbi**, Michael McIntyre, Output Feedback Control of a Single Phase Voltage Source Inverter Utilizing a Variable Structure Observer, *Proceedings of the 2017 American Control Conference, ACC*, Seattle, WA, 2017, pp. 4081-4086.
5. **M. Mohebbi**, M. L. McIntyre, J. Latham and P. Rivera, "A filter-based controller for a buck converter," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-5.
6. P. R. Rivera, M. L. McIntyre, **M. Mohebbi** and J. Latham, "Nonlinear control for single-stage single-phase grid-connected photovoltaic systems*," 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-7.
7. **M. Mohebbi,** M. L. McIntyre, J. Latham and P. Rivera, Nonlinear control of standalone inverter with unbalanced, nonlinear load, *2017 IEEE Power and Energy Conference at Illinois (PECI),* Champaign, IL, USA, 2017, pp. 1-8.

8. **M. Mohebbi**, M. L. McIntyre and J. Latham, A backstepping controller for voltage source inverter with inductor current and output current observers, *2017 IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, USA, 2017, pp. 1-5.
9. **M. Mohebbi**, M. L. McIntyre and J. Latham, A learning backstepping controller for voltage source inverter with nonlinear loads**,** *2017 IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, USA, 2017, pp. 1-5.
10. N. Moghadam, **M. Mohebbi** and H. Li, Opportunistic scheduling for network coded data in wireless multicast networks, *2017 International Conference on Computing, Networking and Communications (ICNC)*, Santa Clara, CA, 2017, pp. 996-1000.
11. J. Latham, M. L. McIntyre and **M. Mohebbi**, Nonlinear adaptive current control for linear vapor compressors, *2016 IEEE International Conference on Automation Science and Engineering (CASE)*, Fort Worth, TX, 2016, pp. 1257-1262
12. **M. Mohebbi,** Florian Luaire, Douglas Jackson, John Naber, Smart Brief for Home Health Monitoring, *UT- KBRIN Bioinformatics Summit 2016*.
13. **M. Mohebbi,** Florian Luaire, Douglas Jackson, John Naber, Smart Brief Monitoring System for Assisted Living, *IEEE International Conference on Consumer Electronics (ICCE),* Las Vegas, NV, 2016, pp. 569-572.
14. **M. Mohebbi,** Michael McIntyre, Joseph Latham, Energy Efficient DC to AC Power Conversion Using Advanced Controllers and Novel Voltage Trajectories, *IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL),* Vancouver, BC, 2015, pp. 1-8.
15. **M. Mohebbi,** Michael McIntyre, Joseph Latham, Vehicle to Grid Utilizing a Backstepping Controller for Bi-Directional Full Bridge Converter and Five Level Active Neutral Point Inverter, *IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL),* Vancouver, BC, 2015, pp. 1-8.
16. Michael McIntyre, **M. Mohebbi,** Joseph Latham, Nonlinear Current Observer for Backstepping Control of Buck Type Converters, *IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL),* Vancouver, BC, 2015, pp. 1-8.
17. **M. Mohebbi,** Michael McIntyre, Joseph Latham, A Novel Two Stage DC/AC Power Converter Optimized for Energy Efficiency, *Renewable Energy and Energy Efficiency Workshop 2015.*
18. **M. Mohebbi,** Michael McIntyre, Joseph Latham, Vehicle to Grid Utilizing a Backstepping Controller for DC/DC Full Bridge Converter and Five Level Active Neutral Point Clamped DC/AC Inverter, *Renewable Energy and Energy Efficiency Workshop 2015.*
19. **M. Mohebbi,** Michael McIntyre, John Naber, 13.8 KV Five Level ANPC Inverter for Wind Power*, IEEE Energy Conversion Congress and Exposition (ECCE*), Pittsburgh, PA, 2014, pp. 4606-4611.
20. **M. Mohebbi**, N. Moghadam, H. Li, L. Cao, R. Visawanathan, Resource Allocation Schemes for Minimum BER Transmission in OFDM Systems, *2014 Integrated Communications, Navigation and Surveillance Conference (ICNS) Conference Proceedings,* Herndon, VA, 2014, pp. M3-1-M3-8.

21. **M. Mohebbi**, V.T. Vakili, A New Scheme for Signal Reception in Space Time Block Coded MC-CDMA, *Second IFIP International Conference on Wireless and Optical Communications Networks, 2005. WOCN 2005*, 2005, pp. 463-467.
22. **M. Mohebbi**, Adaptive Phase Meter, *Iranian Student Conference on Electrical Engineering ISCEE 2002, Shiraz.*

ADVANCED TRAINING

- Certificate of Graduate Teaching Assistant Academy, University of Louisville, 2016-2017.
- Electric Power Distribution Systems, Electric Power Research Institute (EPRI), 2015.
- Failure Mode and Effect Analysis (FMEA), TUV NORD Academy, 2008.

ORGANIZATIONS:

- Member of the GEARED Student Innovation Board representing the University of Louisville
- Institute of Electrical and Electronics Engineers (IEEE)
- International Society of Automation (ISA)
- Kentucky Academy of Science (KAS)

SERVICE

- Paper Reviewer, Power and Energy Conference at Illinois, PECI, 2017.
- Paper Reviewer, American Control Conference, ACC, 2017.
- Paper Reviewer, Springer, Energy Systems, 2015.
- Held a Workshop for Automation and PLC, University of Louisville, 2015.
- Statistical Analysis for Identifying Patients at High Risk for Heart Failure Readmission, Pathology Department, University of Louisville, 2015.
- Paper reviewer, Wireless Networking Symposium, Globecom, 2013.
- Director of Student Science Association of Amirkabir University of Technology, Tehran, 2001.
- Coordinator of the Iranian Student Conference on Electrical Engineering, ISCEE, Shiraz, 2002.